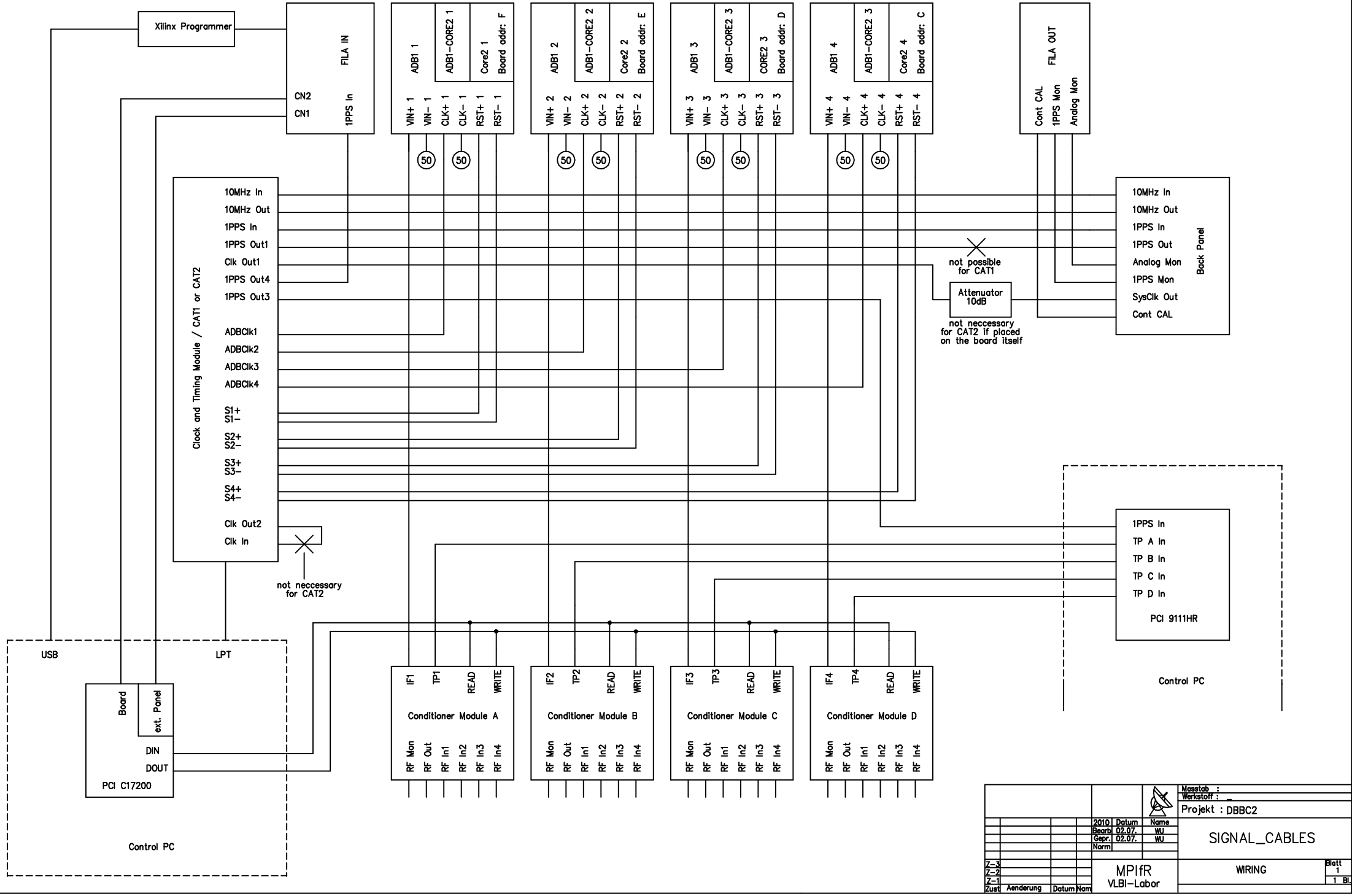
Xilinx Programmer
FILA IN
CN2
CN1
1PPS In
ADB1 1
ADB1-CORE2 1
Core2 1
Board addr: F
VIN+ 1
VIN- 1
CLK+ 1
CLK- 1
RST+ 1
RST- 1
ADB1 2
ADB1-CORE2 2
Core2 2
Board addr: E
VIN+ 2
VIN- 2
CLK+ 2
CLK- 2
RST+ 2
RST- 2
ADB1 3
ADB1-CORE2 3
CORE2 3
Board addr: D
VIN+ 3
VIN- 3
CLK+ 3
CLK- 3
RST+ 3
RST- 3
ADB1 4
ADB1-CORE2 3
Core2 4
Board addr: C
VIN+ 4
VIN- 4
CLK+ 4
CLK- 4
RST+ 4
RST- 4
FILA OUT
Cont CAL
1PPS Mon
Analog Mon
50
Clock and Timing Module / CAT1 or CAT2
10MHz In
10MHz Out
1PPS In
1PPS Out1
Clk Out1
1PPS Out4
1PPS Out3
ADBClk1
ADBClk2
ADBClk3
ADBClk4
S1+
S1-
S2+
S2-
S3+
S3-
S4+
S4-
Clk Out2
Clk In
not neccessary for CAT2
not possible for CAT1
Attenuator 10dB
not neccessary for CAT2 if placed on the board itself
Back Panel
10MHz In
10MHz Out
1PPS In
1PPS Out
Analog Mon
1PPS Mon
SysClk Out
Cont CAL
1PPS In
TP A In
TP B In
TP C In
TP D In
PCI 9111HR
Control PC
USB
LPT
Board
ext. Panel
DIN
DOUT
PCI C17200
Control PC
IF1
TP1
READ
WRITE
Conditioner Module A
RF Mon
RF Out
RF In1
RF In2
RF In3
RF In4
IF2
TP2
READ
WRITE
Conditioner Module B
IF3
TP3
READ
WRITE
Conditioner Module C
IF4
TP4
READ
WRITE
Conditioner Module D
Masstab :
Werkstoff :
Projekt : DBBC2
2010 Datum Name
Bearb 02.07. WU
Gepr. 02.07. WU
Norm
SIGNAL_CABLES
Z-3
Z-2
Z-1
Zust Aenderung Datum Nam
MPIfR
VLBI-Labor
WIRING
Blatt 1
1 Bl.