DBBC3 – Status

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DBBC (Digital Base Band Converter) family overview:

- VLBI back-ends
- VSI to network converters
- VLBI data buffers / post-processing units

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DBBC Back-end: past to present

DBBC1 2004 - 2008

in: 4 x IF-512MHz

out: **DDC** 16 x bbc (1-2-4-8-16MHz)@32MHz

0.512/1.024 Gbps

DBBC2 2007 – today

in: 4 x IF-512/1024MHz

out: **DDC** 16 x bbc (1-2-4-8-16-32MHz)@32/64MHz

PFB 4 x 16 x (32-64 MHz)@64/128MHz

4.096/8.192 Gbps

DBBC2010 2009 – today

in: 8 x IF – 512/1024MHz

out: **PFB** / **DSC** **16.384/32.768 Gbps**

The development of the DBBC3 is aimed at:

Astronomy

- **EVN wide-band VLBI backend (≤ 32 Gbps)**
- **EHT (Event Horizon Telescope) (≤ 64 Gbps)**

Geodesy

- **VGOS ultra-wide-band VLBI system (≤ 32 Gbps)**

Supported by RadionNet3: JRA DIVA

DBBC Back-end: present

DBBC3L (-2L2L) **EVN32Gbps / EHT / GMVA ...**

in: 2 x IF-4096 / 4 x IF-2048 / 8 x IF-1024

out: **DDC** 1-2-4-8-16-32-64-128-256 MHz

PFB 32 - 64 -128 - 256 MHz

DSC 1024 - 2048 - 4096 MHz

≤16/32 Gbps

DBBC3L (-4L4H) **VGOS / EHT w. ALMA**

in: 4 x IF-4096 / 8 x IF-2048 / 16 x IF-1024

out: **DDC** 1-2-4-8-16-32-64-128-256 MHz

PFB 32 - 64 -128 - 256 MHz

DSC 1024 - 2048 - 4096 MHz

≤ 16/32/64 Gbps

DBBC Back-ends: present to future

DBBC3L (-8L8H)

in: 8 x IF-4096 / 16 x IF-2048 / 32 x IF-1024 MHz

out: **DDC** 1-2-4-8-16-32-64-128-256 MHz

PFB 32 - 64 -128 - 256 MHz

DSC 1024 - 2048 - 4096 MHz

≤16/32/64/128 Gbps

DBBC3H (-2H2H/-4H4H) 2016 **VGOS full-compliant**

in: 4 x IF-14336 MHz

out: **DDC** 1-2-4-8-16-32-64-128-256-512-1024 MHz

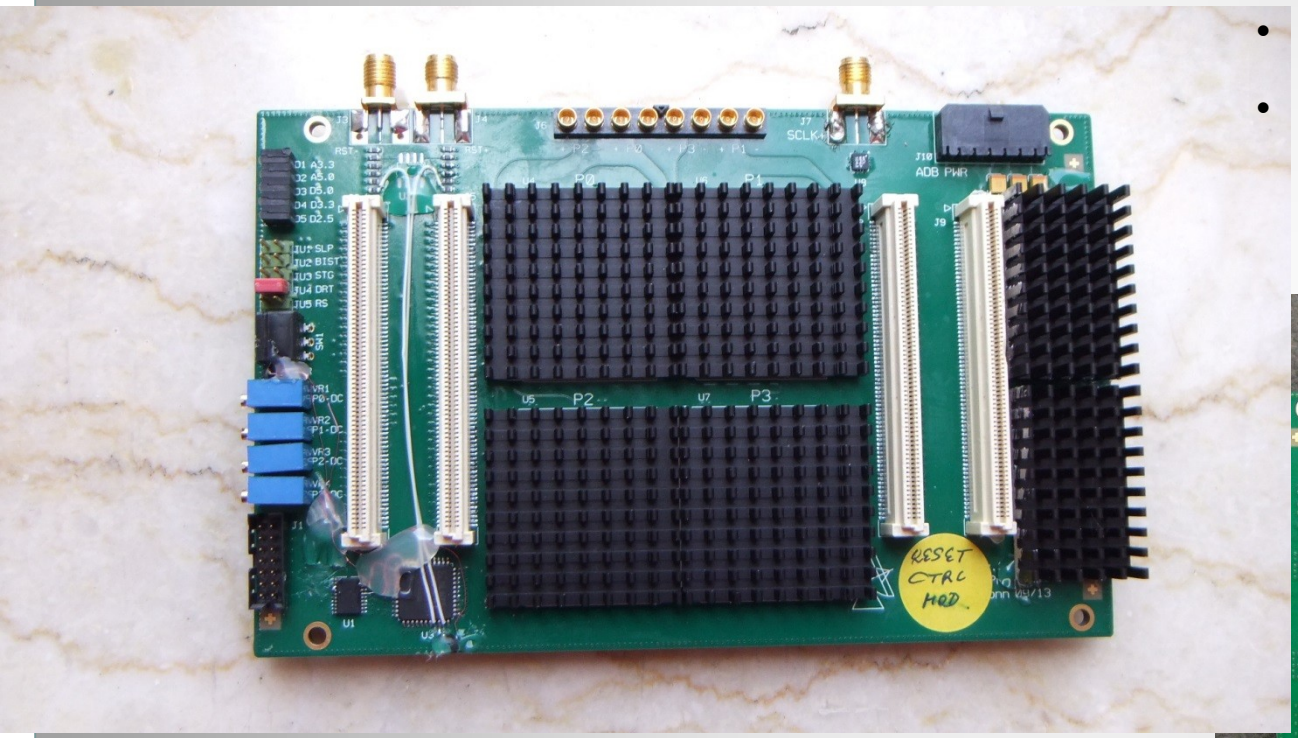
PFB 32-64-128-256-512-256-512-1024 MHz

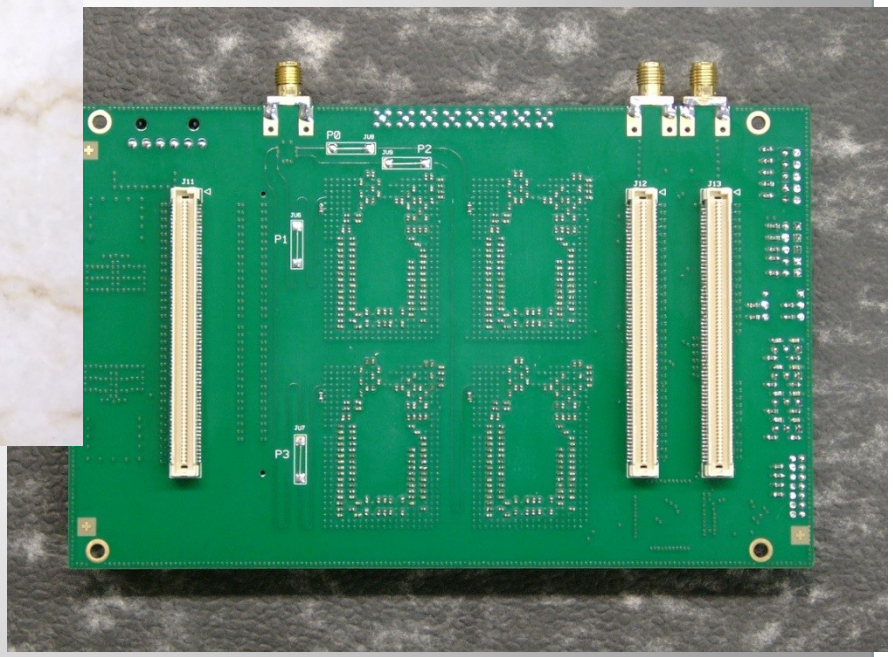
DSC 1024-2048-4096-8192-14336 MHz

≤16/32/64/128/229 Gbps

ADB3L

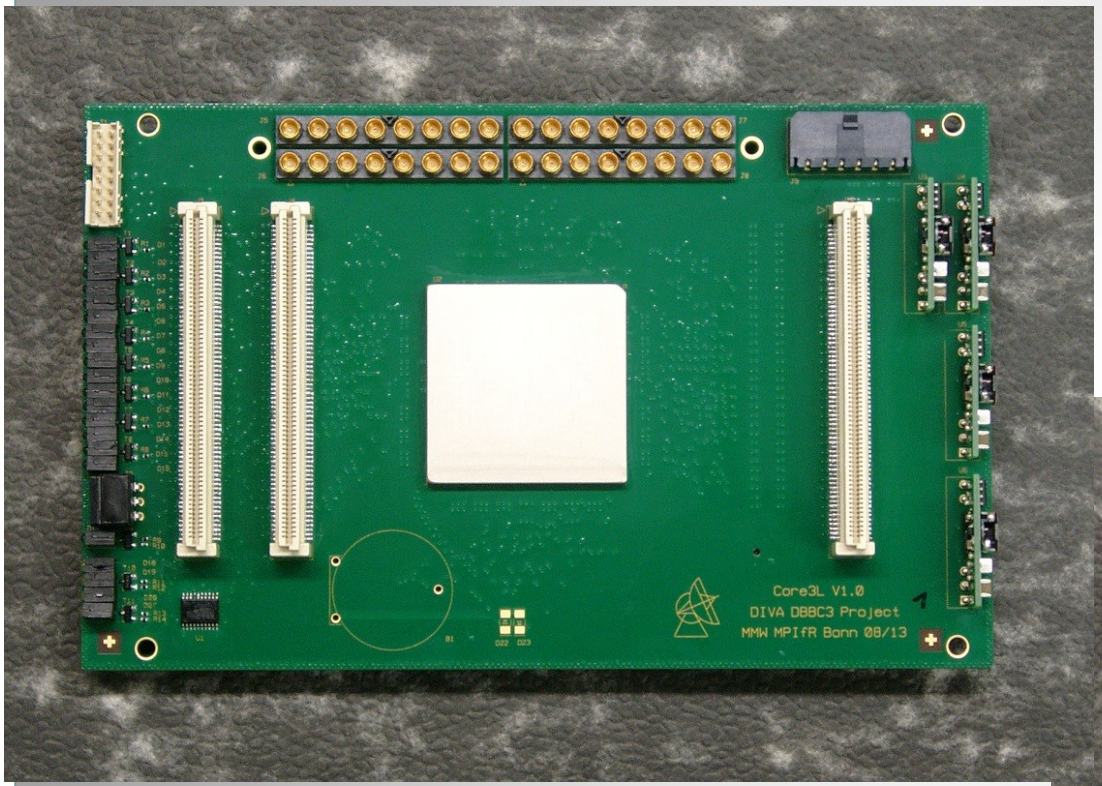
- Number of IFs: **1 - 4**
- Equivalent Sample Rate IF: **8 GSps**
- Instantaneous bandwidth: **4 GHz**
- Sampling representation: **10 bit**
- Real/Complex Sampling
- Compatibility with existing DBBC

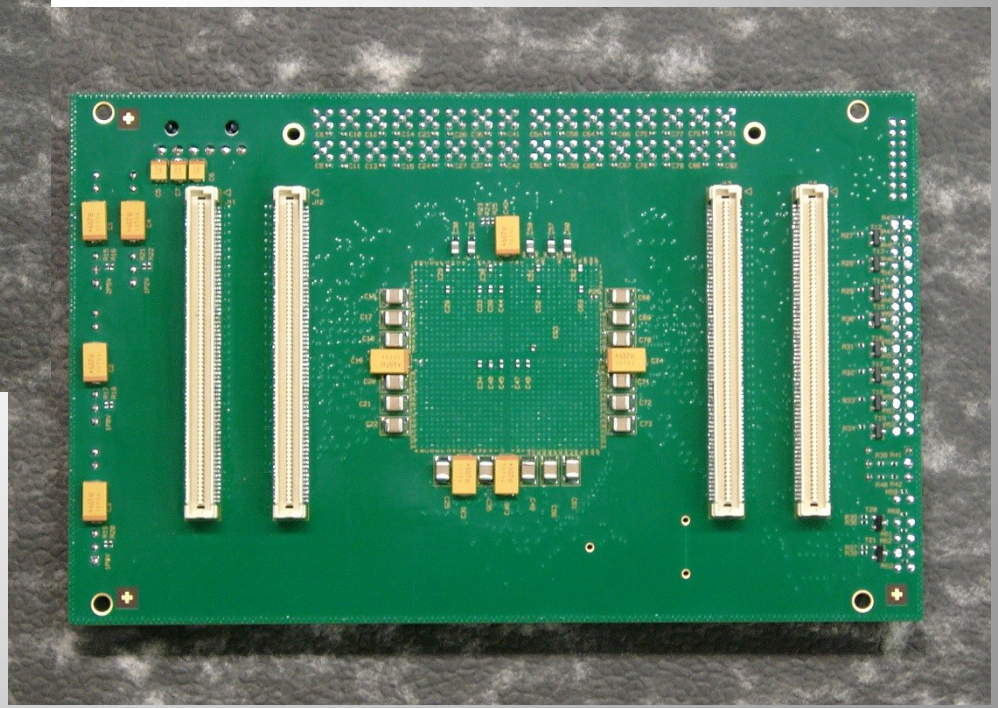




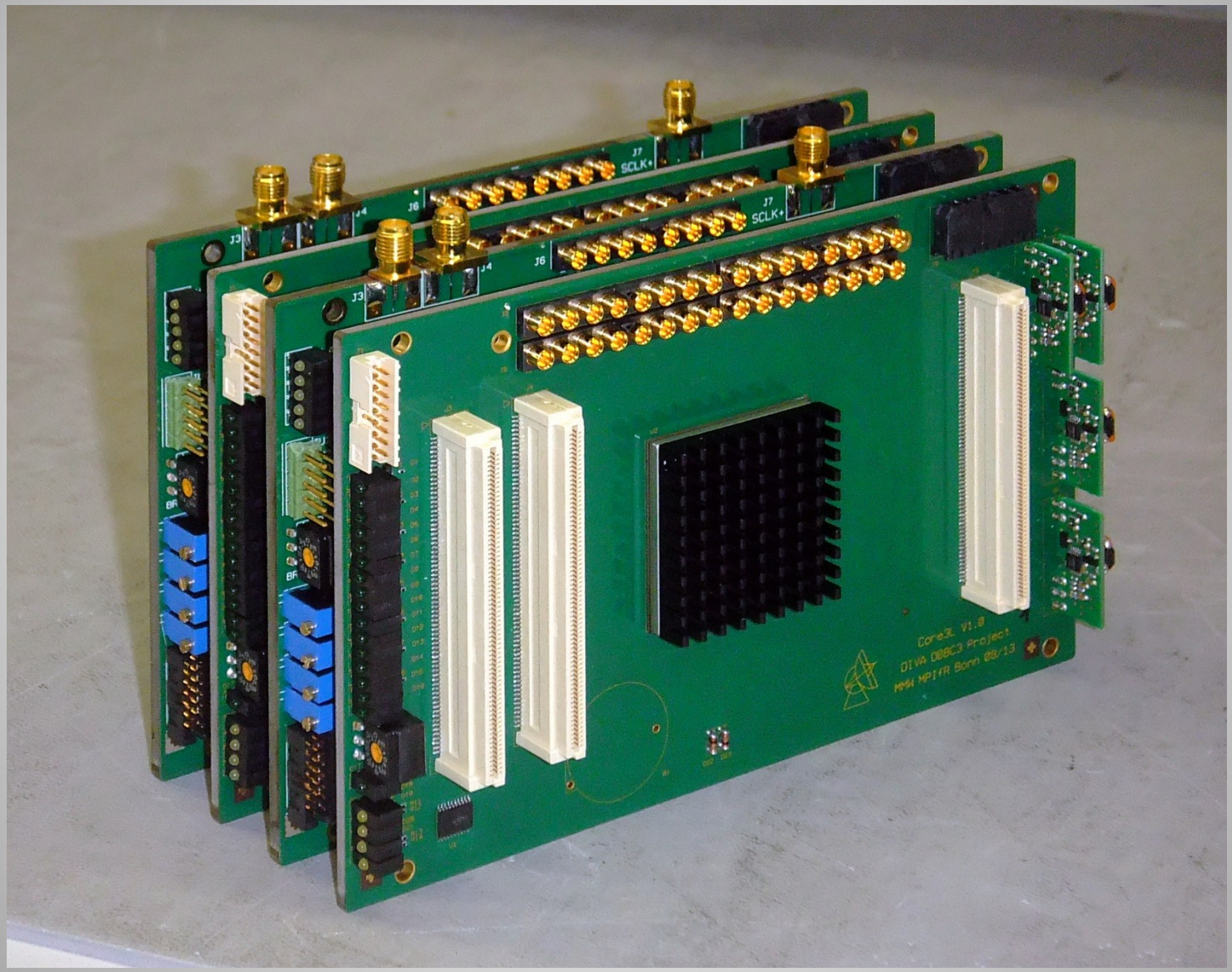
CORE3L

- Input bus: **HSI & HSI2**
- Input sampling representation: **8-10 bit**
- Input bandwidth : **1 x 4GHz, 2 x 2GHz, 4 x 1GHz**
- Processing capability: **DDC, PFB, DCS**
- Output bus: **HSO**
- Output bus mode: **DDR VSI-H**
- Inter-board bus: **4 Input + 4 output Cu 10GE**
- Compatibility with existing DBBC environment

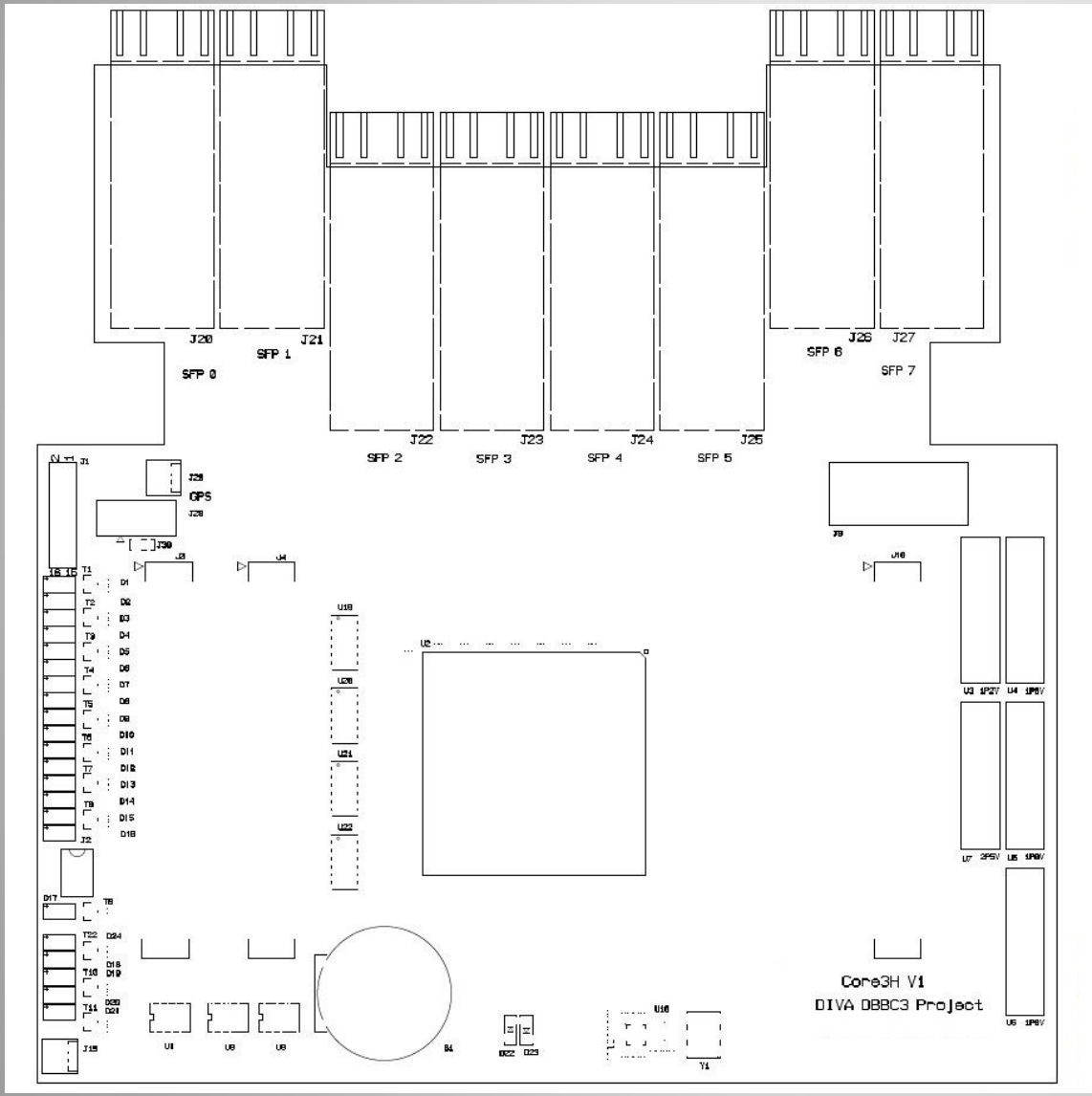




Stack with 2 ADB3L and 2 CORE3L
4 GHz bwd dual polarization

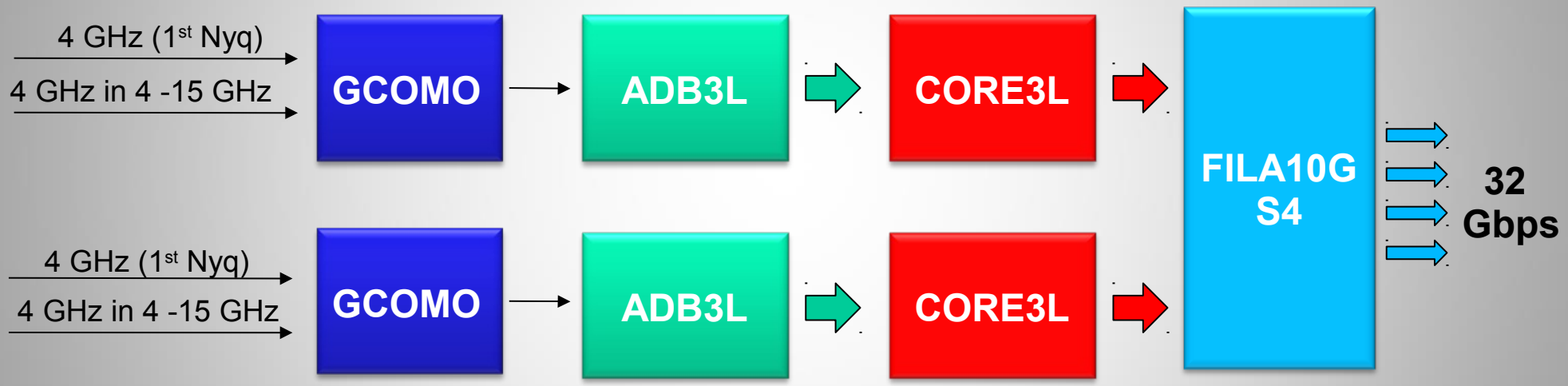


CORE3H



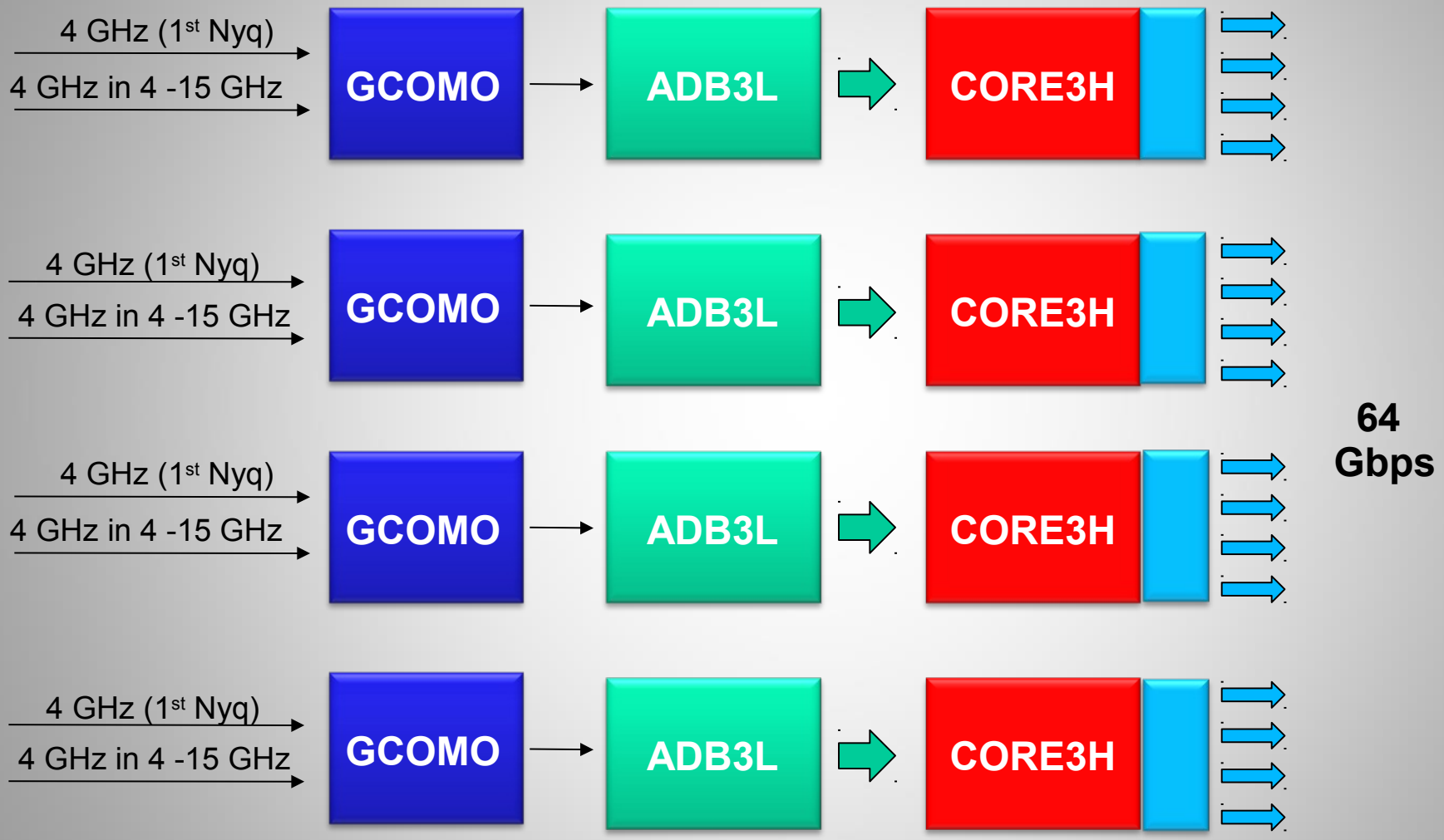
- Input bus: **HSI & HSI2**
- Input sampling representation: **8-10 bit**
- Input bandwidth : 1 x **4GHz, 2 x 2GHz, 4 x 1GHz**
- Processing capability: **DDC, PFB, DCS**
- Output: **8 x 10GE SFP+**
- Inter-board bus: **8 Input 10GE SFP+**
- Compatibility with existing DBBC environment

DBBC3L-2L2L Architecture

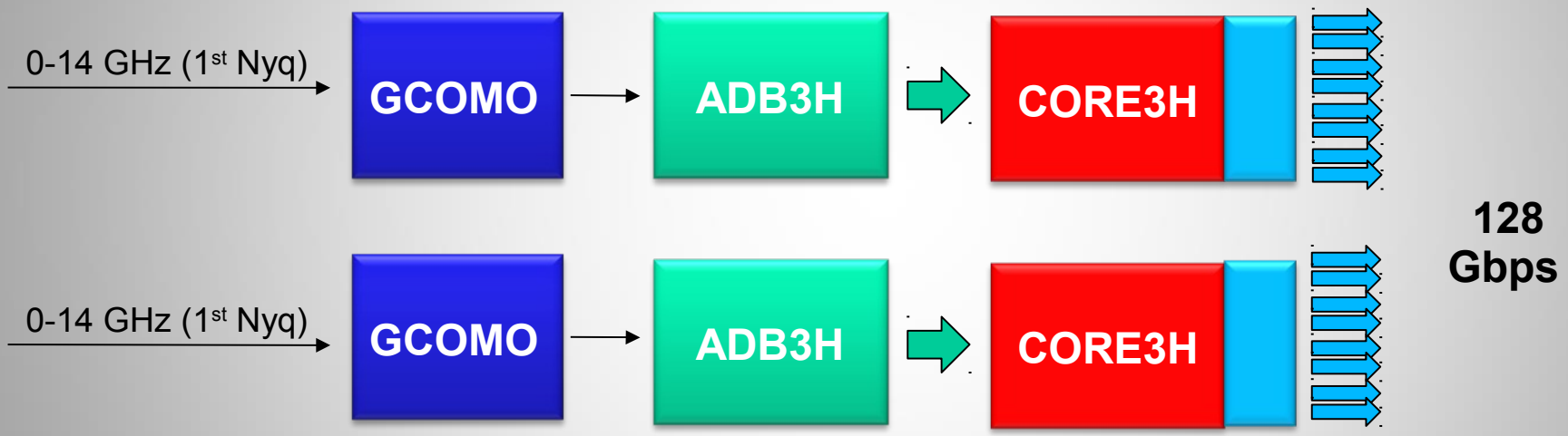


"DIVA DBBC3" presently under field test

DBBC3L-4L4H Architecture



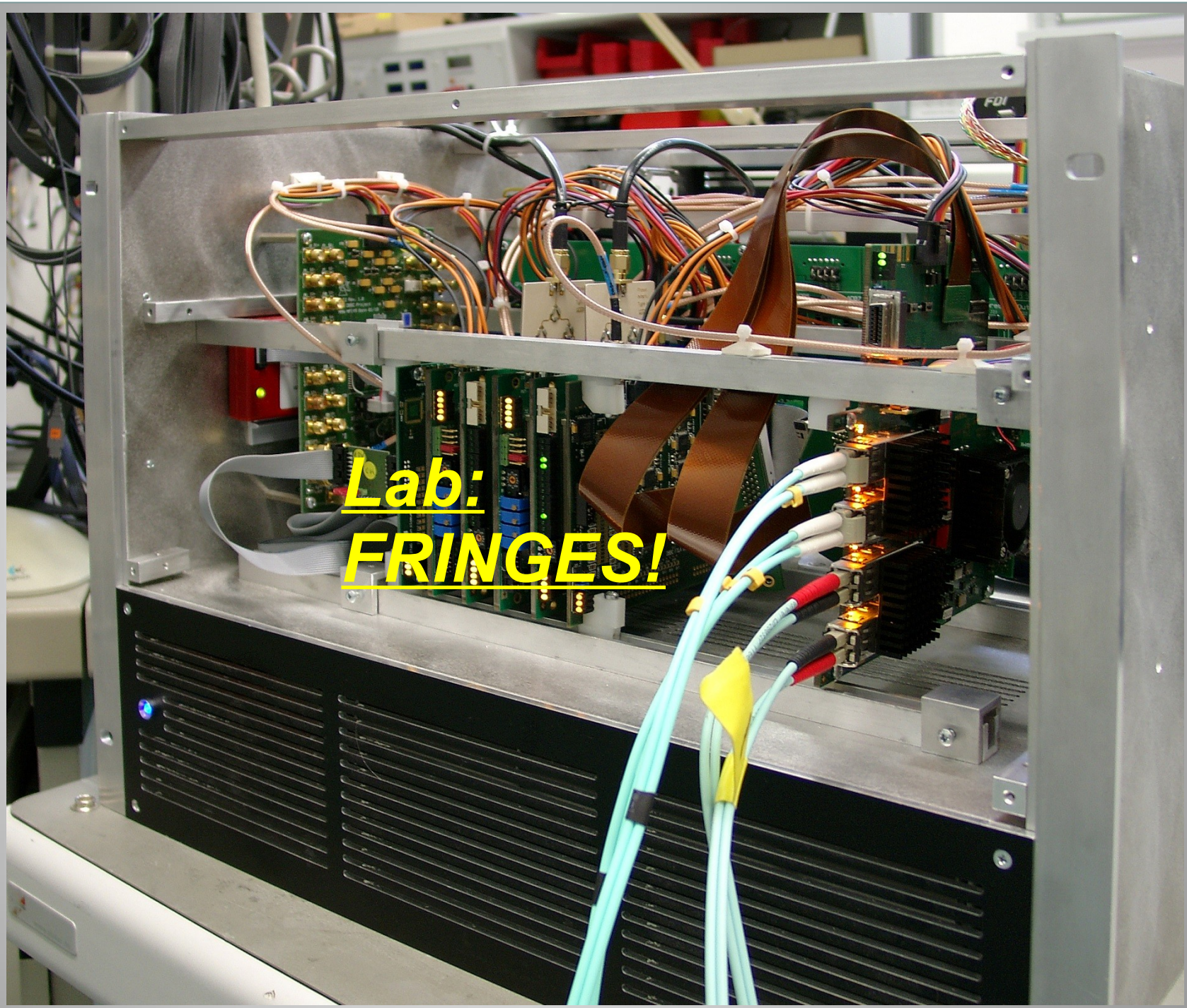
DBBC3H-2H2H Architecture




D B B C 3
EUROPEAN VLBI NETWORK
RadioNet

DBBC3L -2L2L

DBBC3L -2L2L



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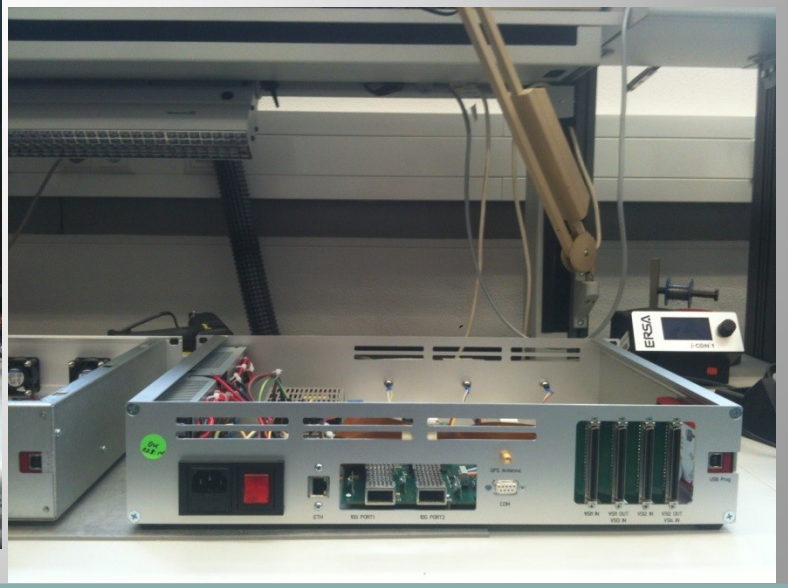
- VLBI data buffers / post-processing units

FILA10G

Shifts VLBI data on Internet – 16 Gbps

4 x VSI-H <> 2 x 10GE

- MK5B up to 4 Gbps
- VDIF Single Thread up to 8Gbps/10G port
- VDIF Multiple Threads
- RAW (no headers)
- Threads eventually corner-turned
- The 10G Ethernet ports independent in destination address in VDIF-ST and MK5B
- Multi-thread mode supports an independent block of destination addresses
- Decimation and bit-mask selectable



FILA10G-S4

Shifts VLBI data on Internet – 32 Gbps

8 x VSI-H <> 4 x 10GE

- MK5B up to 4 Gbps
- VDIF Single Thread up to 8Gbps/10G port
- VDIF Multiple Threads
- RAW (no headers)
- Threads eventually corner-turned
- The 10G Ethernet ports independent in destination address in VDIF-ST and MK5B
- Multi-thread mode support an independent block of destination addresses
- Decimation and bit-mask selectable

DBBC (Digital Base Band Converter) family overview:

VLBI back-ends

VLBI network shifters

VLBI data buffers / post-processing units

FILA40G

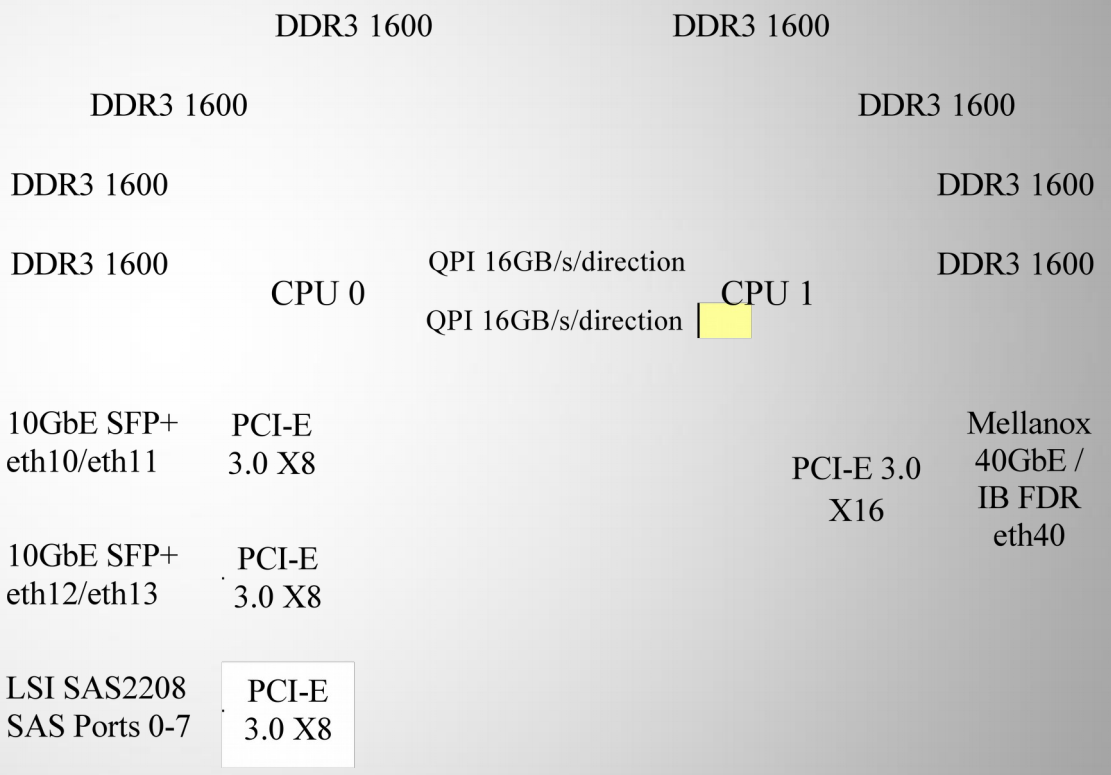
Developed for DBBC3:
Ethernet in/out plus other functions

FILA40G General Key features

- 4 x 10GE Inputs
- 1 x 40GE Output
- Stream aggregation (2/4 threads are cumulated in single thread)
- Format conversion/VDIF threading
- Packet filtering
- Pulsar gating
- Timekeeping via NTP and/or GPS module
  - Propagates UTC to other connected devices via DBBC Local Network (DLN)
- Optional disk storage
  - Expected to record at 32Gbps sustained
  - Compatibilty with Mark6 disk packs/chassis being investigated

FILA40G Architecture for 32 Gbps

- 2 x Intel Xeon E5-2670
  - 8 core 2.60 GHz
- 8 x 8GB DDR3 1600
- 8 Onboard SAS2 ports
- 4 free PCI 3.0 x8 slots
  - To be used to add extra SAS2/3 ports



DBBC3L – Observation Program

- Starting with June 2015 a regular testing observation program started
- Stations involved Noto - Onsala - Effelsberg
- Initially DSC 4 GHz band mode
- Recording: Noto with FILA40G – Onsala with Flexbuff – Effelsberg with MK6
- Output is VDIF 4 thread interleaved per polarization (16 Gbps per pol)
- Correlation requires some development

THANK YOU!