



*RN3 — WP 11 JRA **DIVA***

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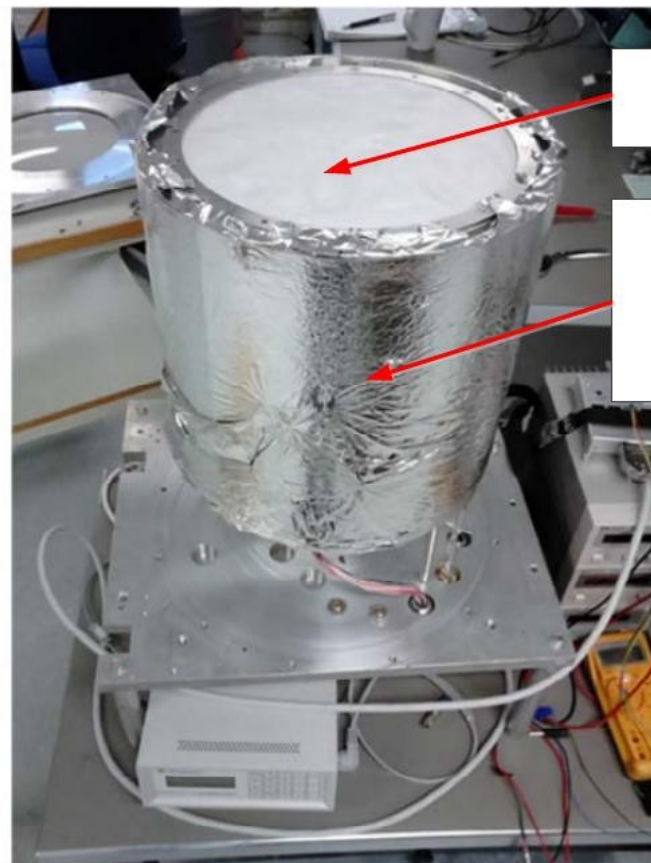
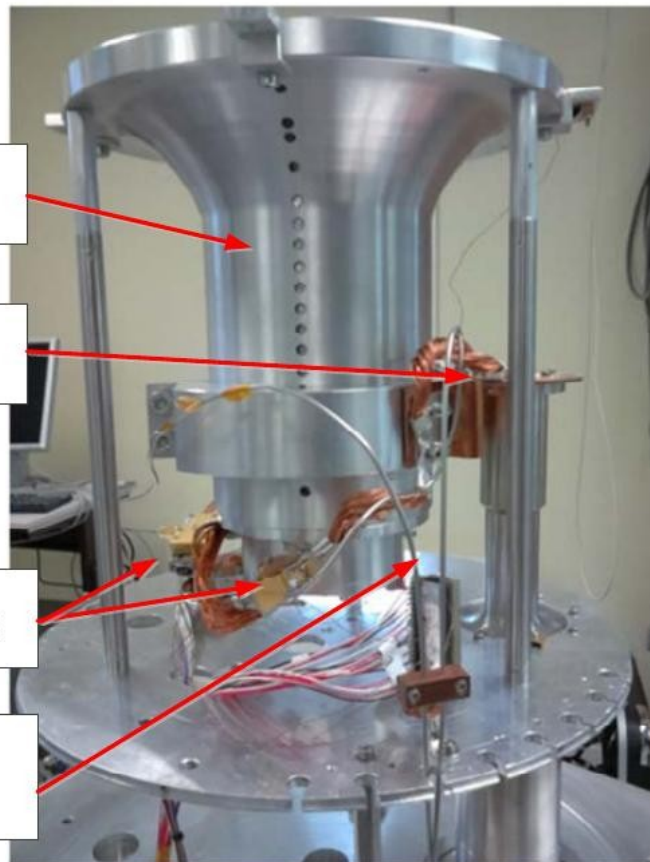


RadioNet3 - **DIVA** – Task 1: wide-band receiver

Two VLBI-related (and SKA-related) Tasks

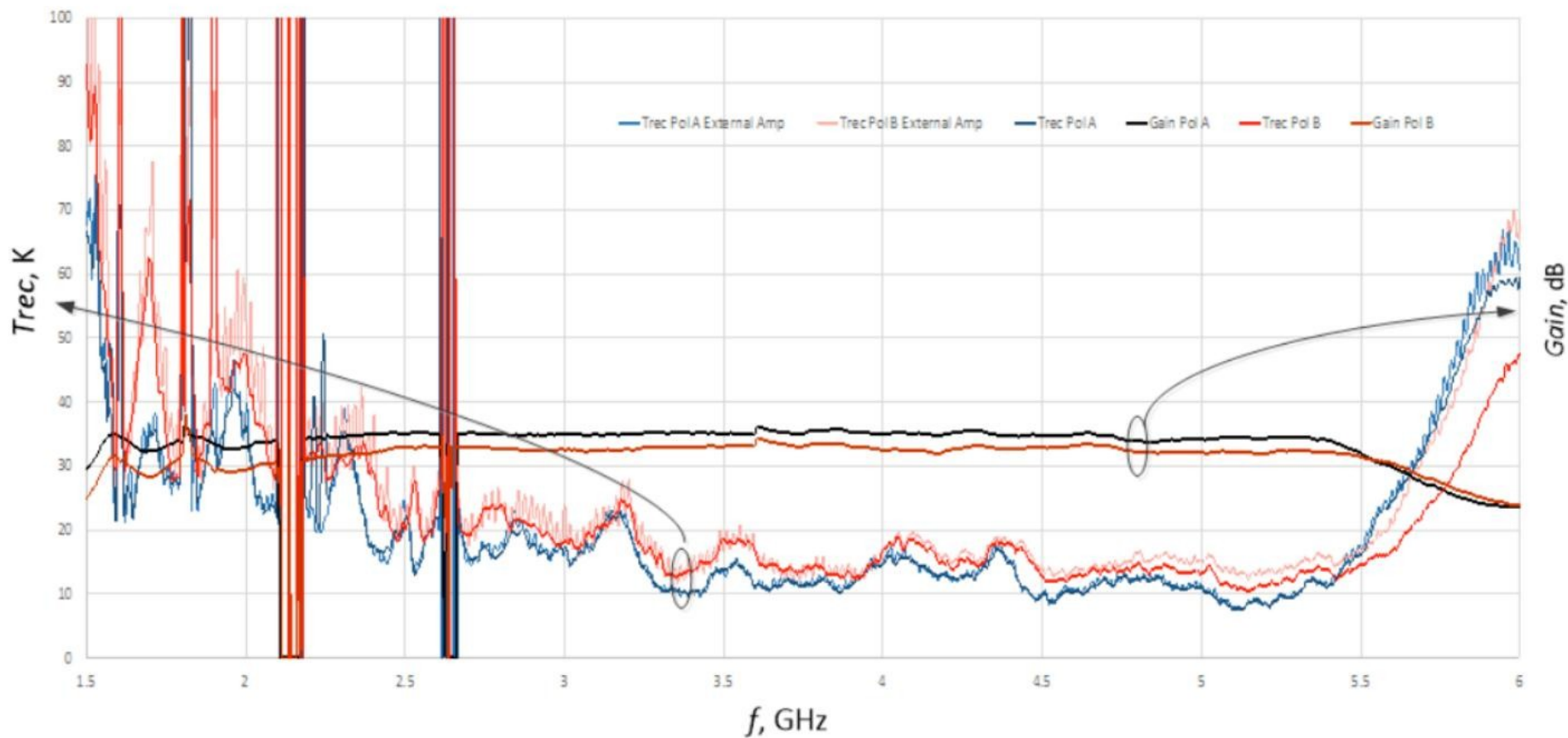
Task 1: Low noise wide-band integrated receiver for VLBI and SKA

- MMIC Design – 1.5 GHz to 5.5 GHz
- Normal machined metal housing for MMIC
- QRFH feed
- Dewar
- Tested in the lab
 - Receiver noise of about 15 K between 3 GHz and 5.5 GHz
- Partners: ASTRON, OSO, MPG, IAF





Power Spectral Density



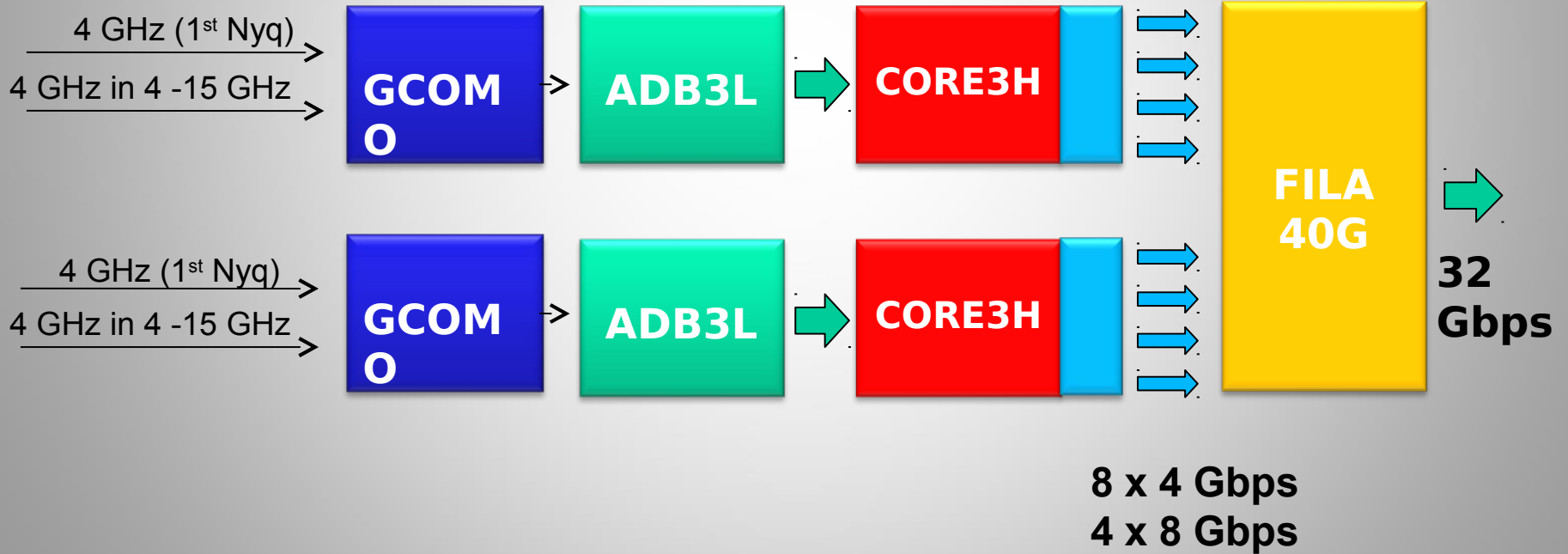


RadioNet3 - **DIVA** – Task 2: DBBC3

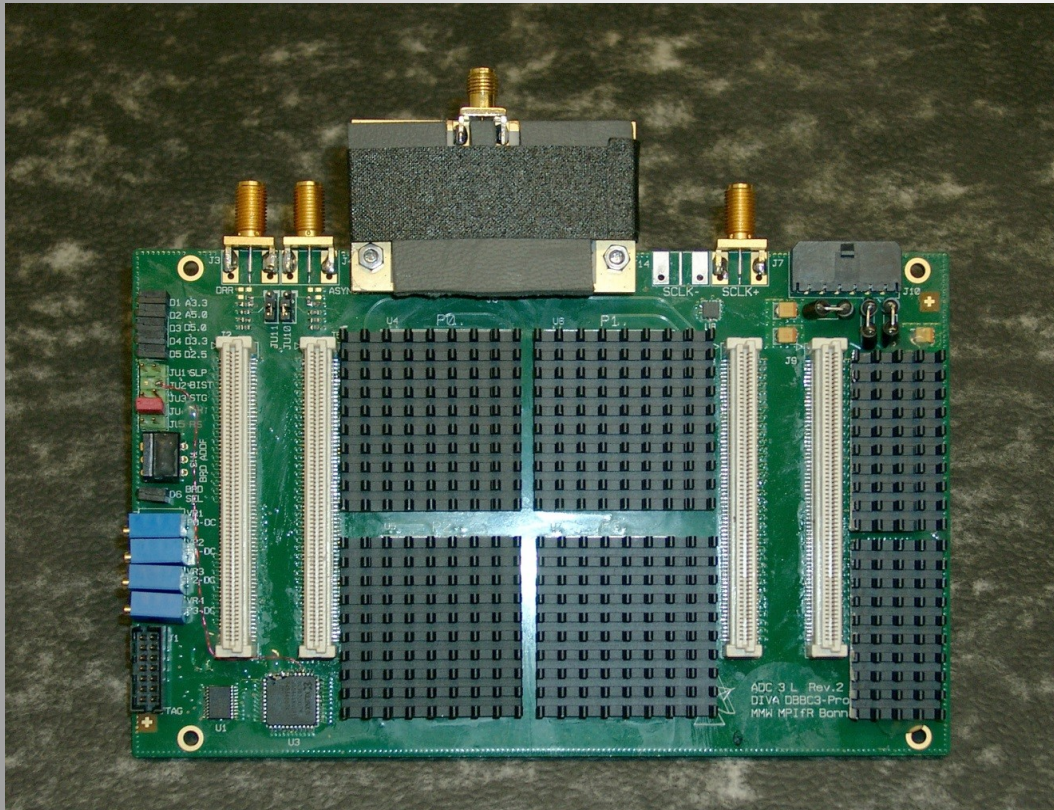
Task 2: DBBC3 VLBI backend (32 Gbps)

- Analogue board with downconverter
- 4 GHz wide ADC (ADB3L) (4x 1GHz interleaved)
- Virtex 7 processing board (CORE3H)
 - “DBBC2 firmware”, wide-band DSC mode, more....
- FiLA40G postprocessor (fast server + disks)
 - VDIF threading, corner turning, decimation,
- Test in lab: zero-baseline
- VLBI: Onsala – Effelsberg (@ 16 Gbps, 1 pol)
- Fringes with OSO DBBC3 to DBBC2s

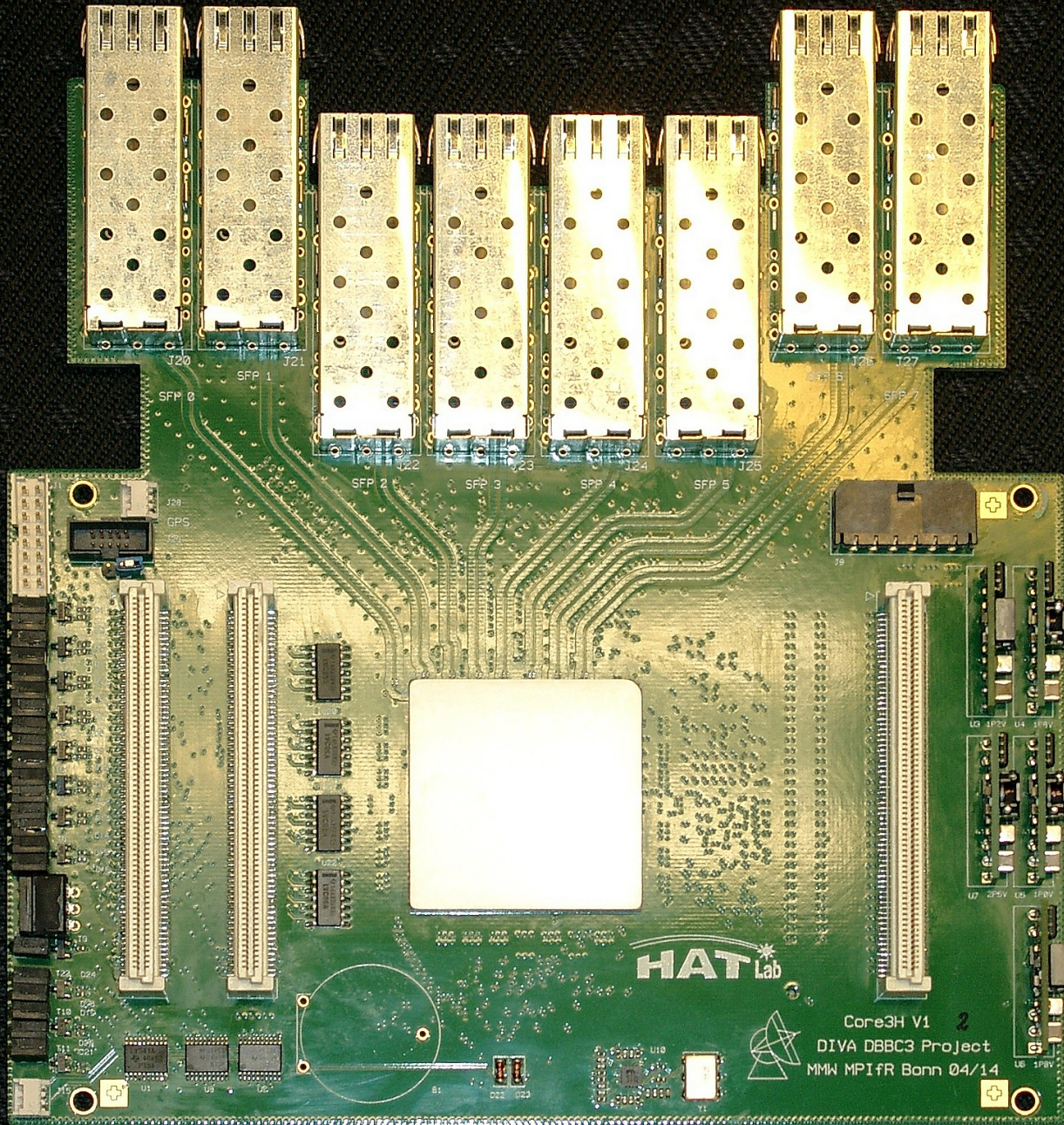
DBBC3L-2L2H Architecture



ADB3L



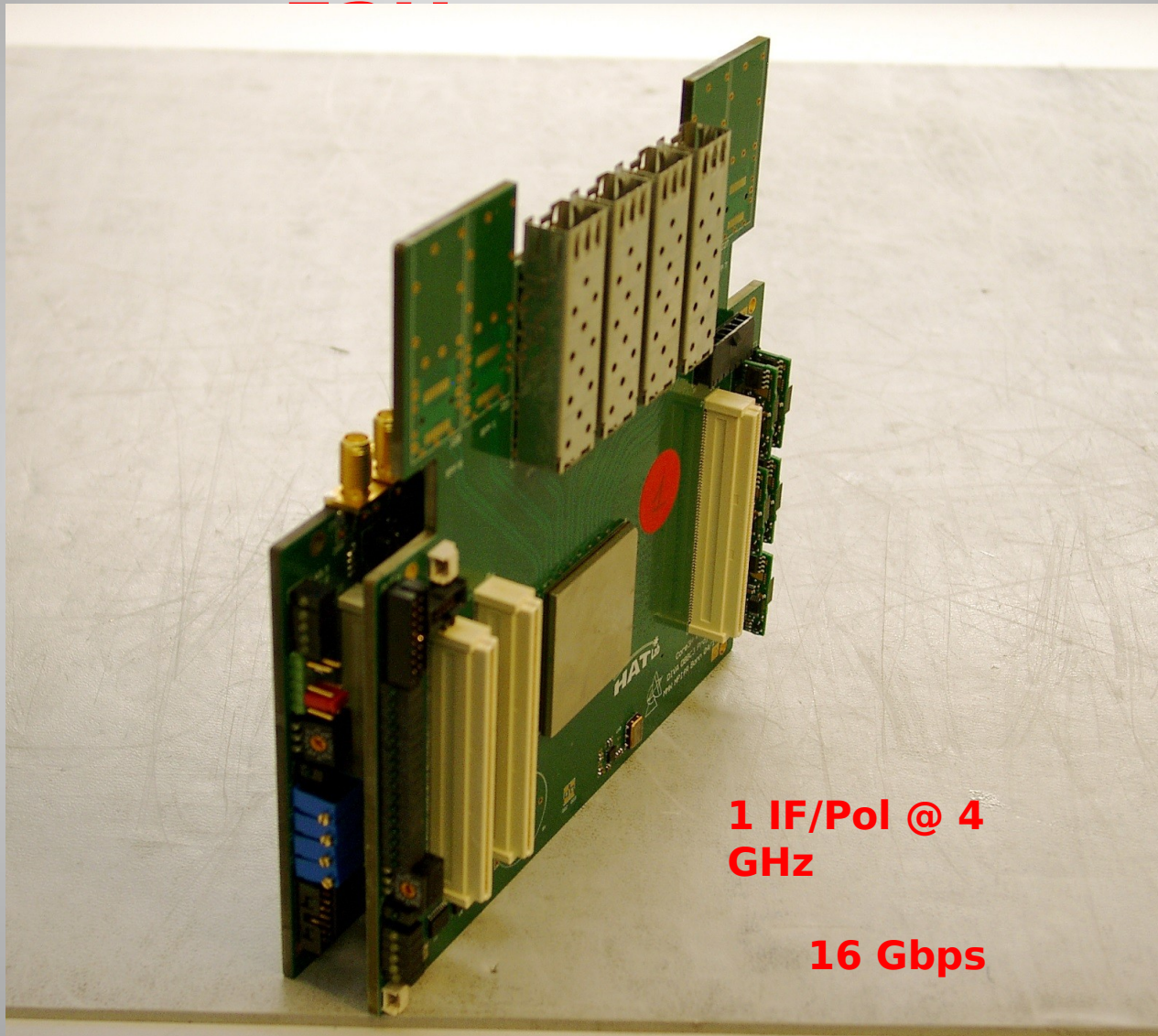
- Number of IFs: **1 - 4**
- Equivalent Sample Rate IF: **8 GSps**
- Instantaneous bandwidth: **4 GHz**
- Sampling representation: **10 bit**
- Real/Complex Sampling
- Compatibility with existing DBBC



HAT Lab

Core3H V1 2
DIVA DBBC3 Project
MMW MPIFR Bonn 04/14

ADB3L+COR



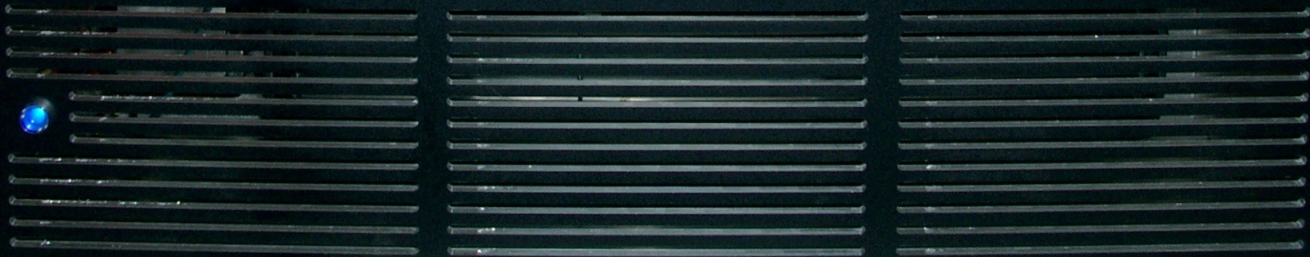
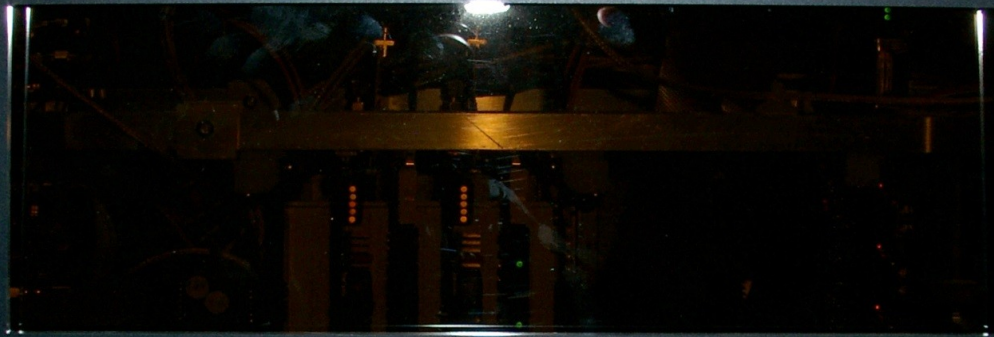
**1 IF/Pol @ 4
GHz**

16 Gbps



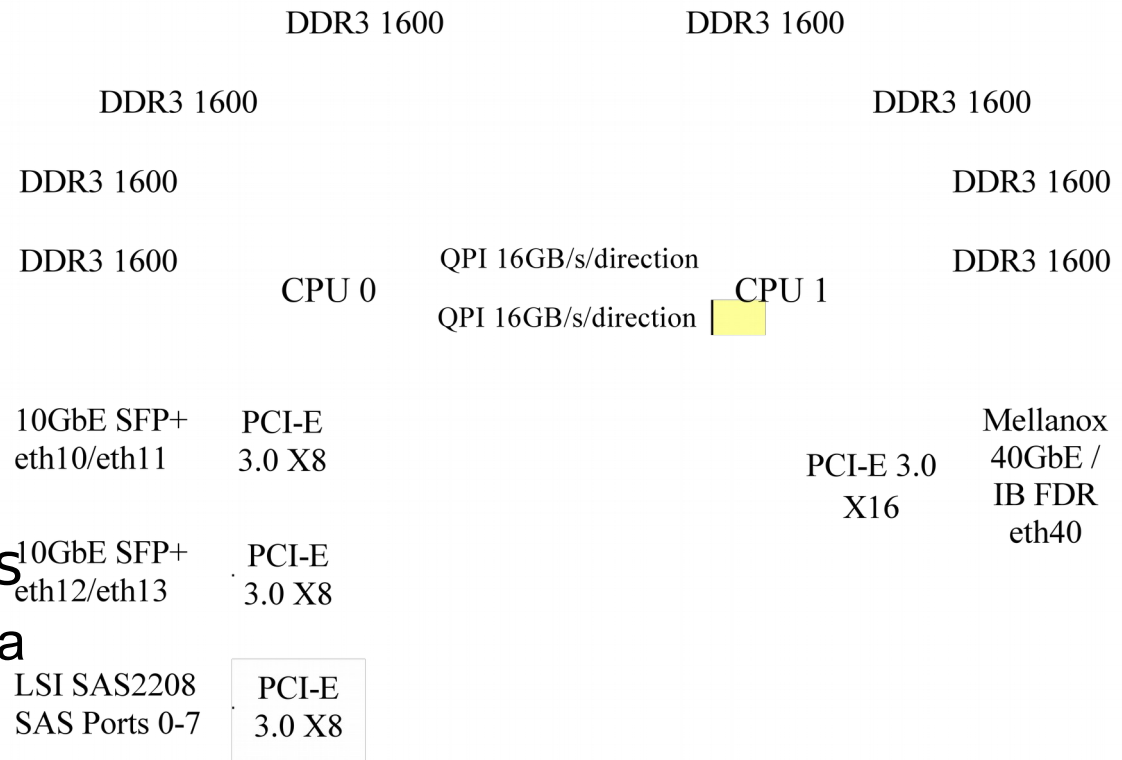


D B B C 3

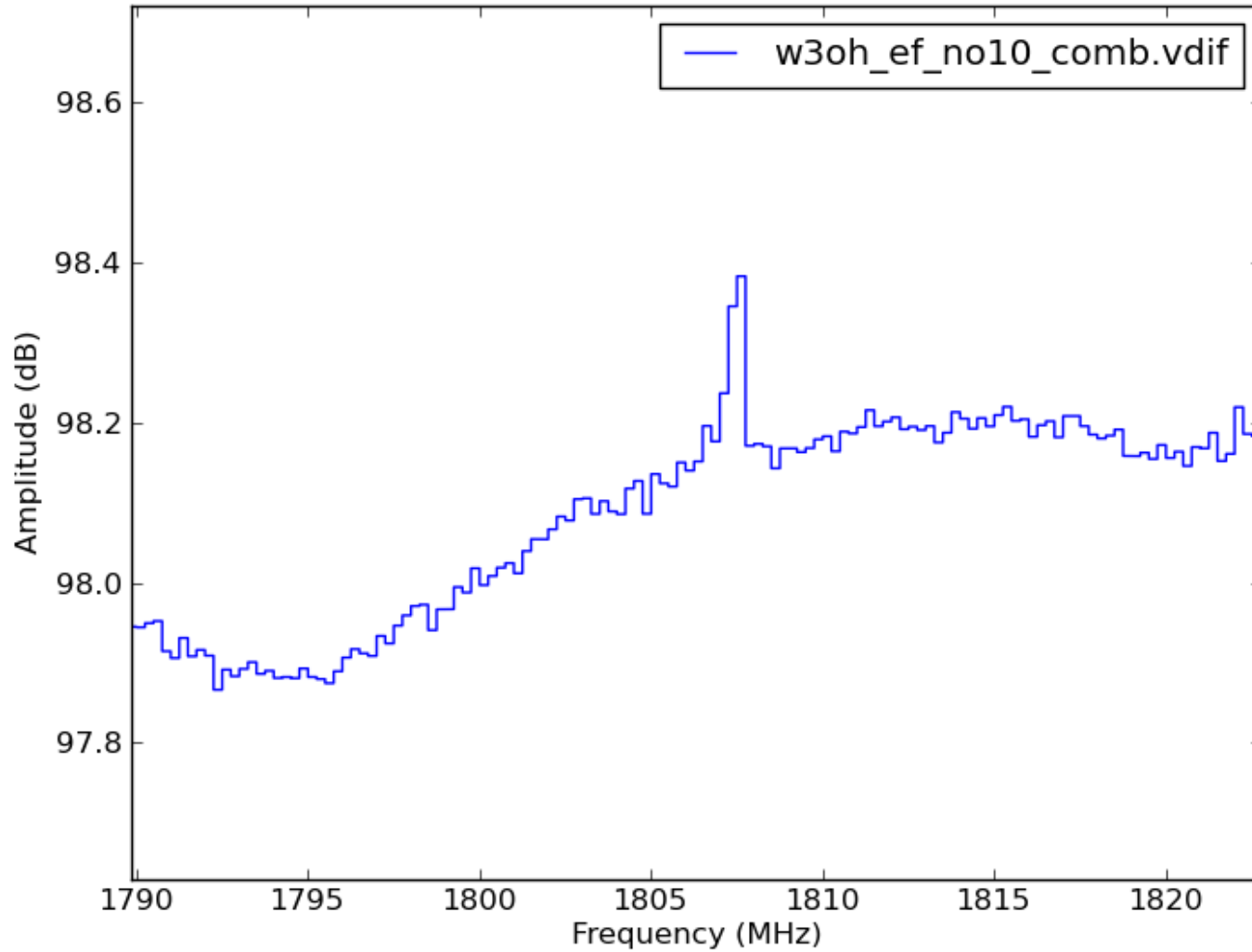


FILA40G Architecture for 32 Gbps

- 2 x Intel Xeon E5-2670
 - 8 core 2.60 GHz
- 8 x 8GB DDR3 1600
- 8 Onboard SAS2 ports
- 4 free PCI 3.0 x8 slots
 - To be used to add extra SAS2/3 ports

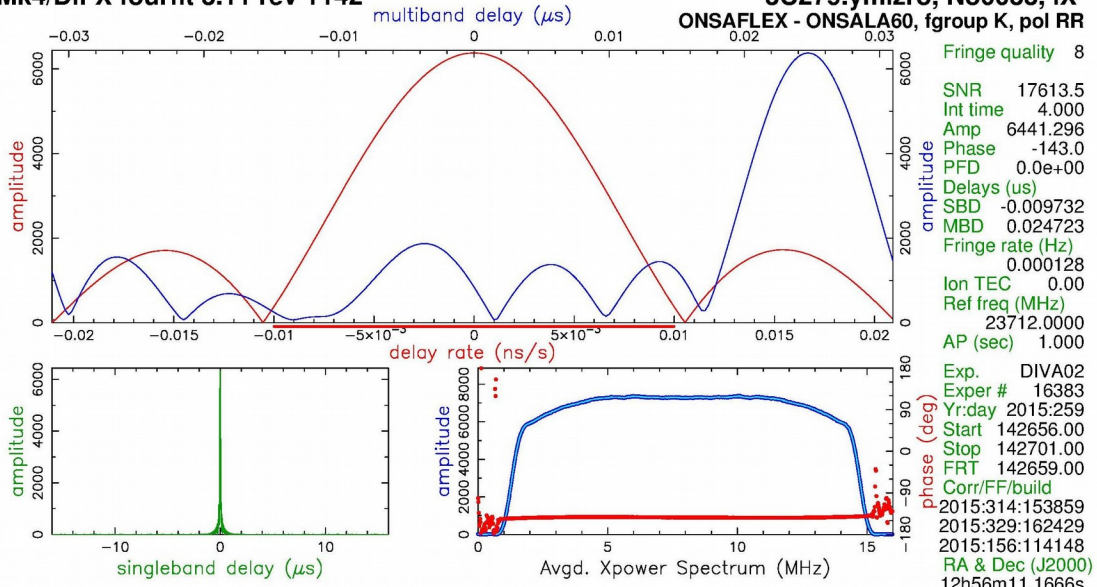


Auto-correlation Amplitudes

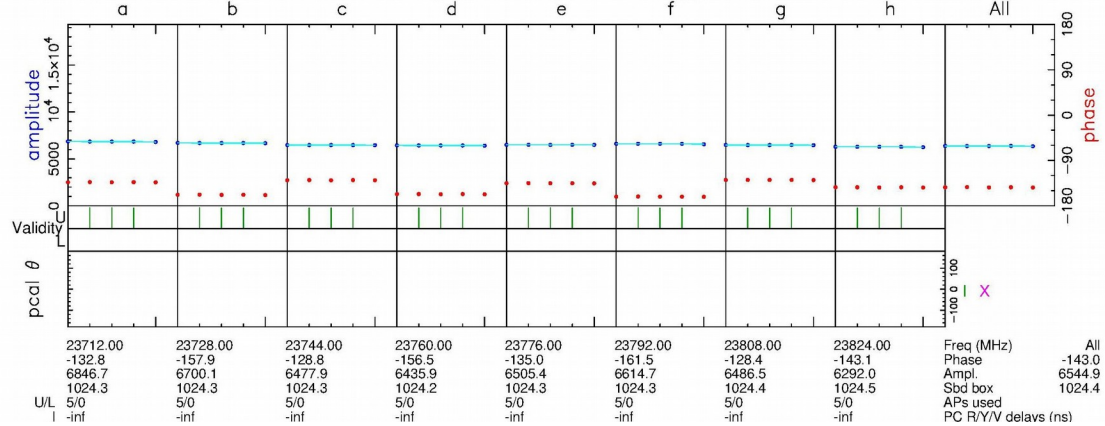


Mk4/DiFX fourfit 3.11 rev 1142

3C279.ymizro, No0033, IX
 ONSAFLEX - ONSALA60, fgroup K, pol RR



Amp. and Phase vs. time for each freq., 5 segs, 1 APs / seg (1.00 sec / seg.), time ticks 1 sec



Firmware under development

- **DSC @4 GHz**
- **PFB @ 256 MHz**
- **DDC @ 128-64-32-16-8 MHz**

.... plus “DBBC2” firmware (partially ported)