

# RDBE / Mark5C

Jon Romney (NRAO)

Chet Ruszczyk (MIT Haystack)

EVN TOG June 21 Helsinki

# Introduction

- RDBE / Mark5C: NRAO / Haystack Joint Project
- RDBE Summary (jon)
- Architecture & PFB bit code (chet)
- Engineering Trials (jon / chet)
- DDC Development (jon)
- Other VLBA Upgrade Topics (jon)
- Mark 5 Update (chet)

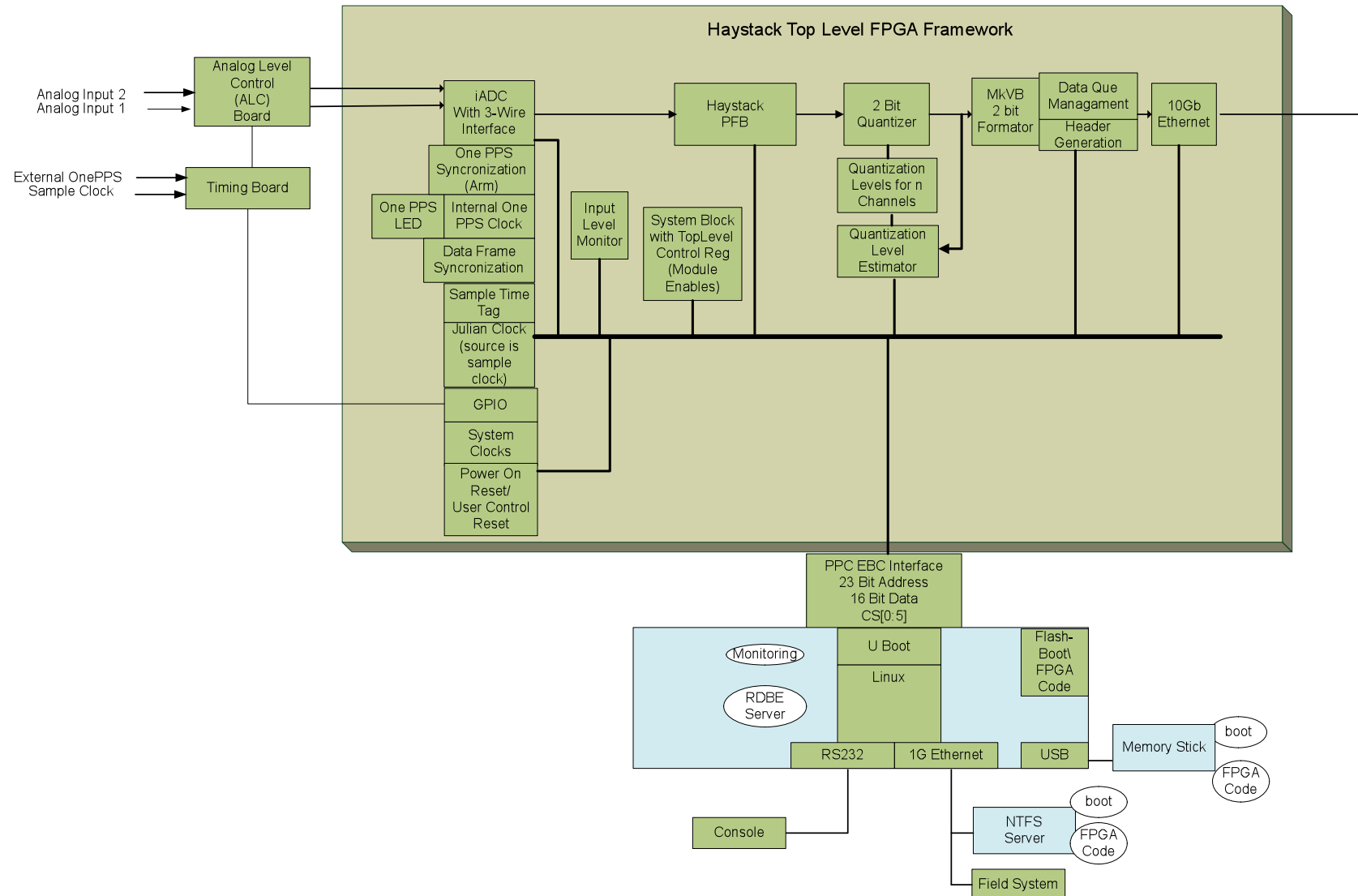
# RDBE Summary (jon)

- Roach Digital Backend
  - Complete system.
    - Includes ROACH, Synthesizer and Analog Level Control (ALC) boards.
  - 3U chassis.
  - Developed by NRAO / Haystack collaboration.
- Based on the ROACH Board
  - “**R**econfigurable **O**pen **A**rchitecture **C**omputing **H**ardware”.
  - Standalone FPGA processing board.
  - Developed by NRAO / KAT / CASPER groups.
- Commercially Available through Digicom
  - About US \$15k.

# Architecture – PFB bit code (chet)

- Specs
  - Polyphase filterbank.
  - 32 x 32-MHz channels.
- Status
  - Works!
  - Common development environment at Haystack & NRAO.
  - Channelization (dual-polar alternate-channels).
- Still to be done:
  - Close level-control loop.
  - Implement switched-power ( $T_s$  measurement).
  - Phase-cal extraction.

# RDBE Bit Code Architecture



# Engineering Trials (jon / chet)

- Zero-baseline bench tests:
  - done (RDBE vs. DBE-1)
- End-to-end Engineering test:
  - done (Wf/Mv3 Baseline – see fringe plot next page)
- VLBI demonstration: Westford – Los Alamos
  - Scheduled July 8<sup>th</sup>
  - RDBE/Mark5C's
  - Correlation
    - Difx (NRAO)
    - MarkIV (Haystack)

# Engineering Trial

Westford:

RDBE/Mark5C

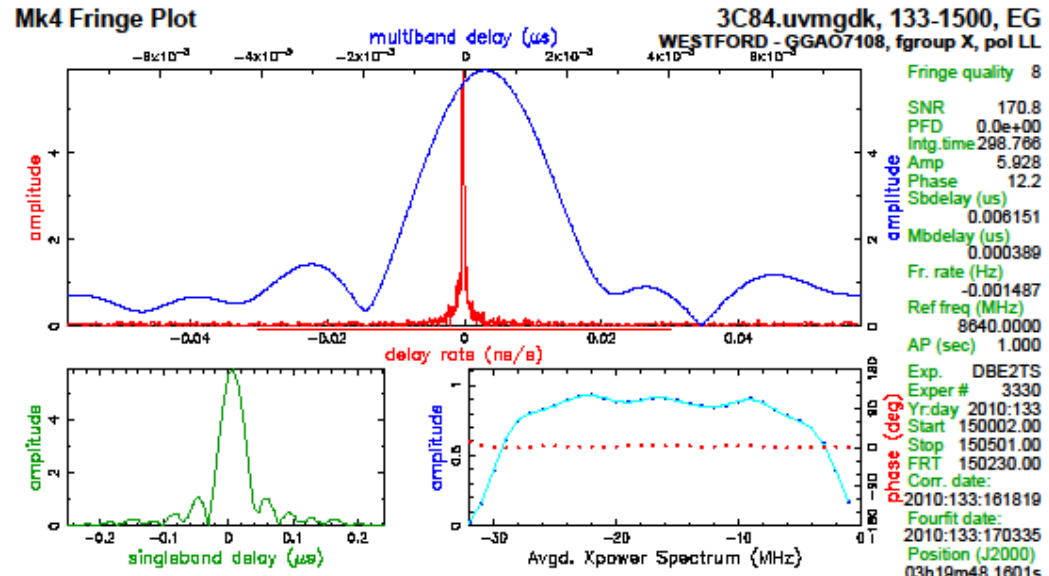
GGAO:

ibob/Mark5B+

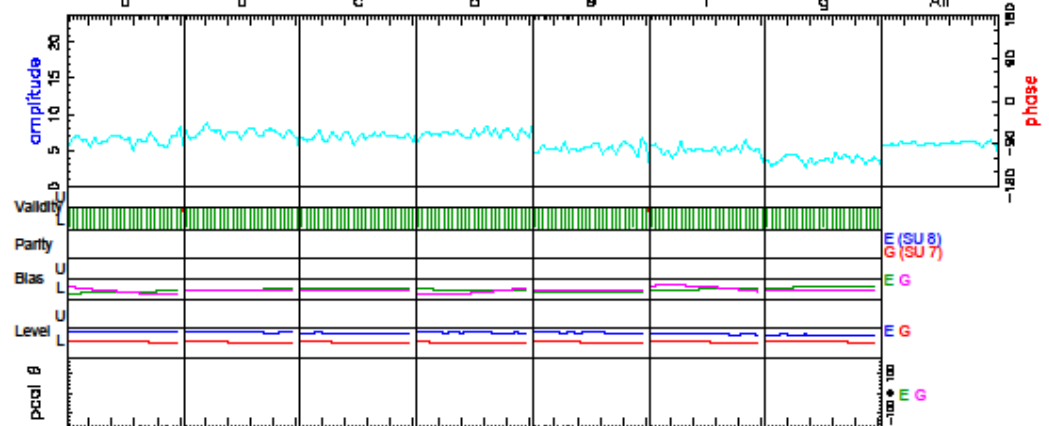
Mark5B Emulation Mode

MarkIV correlator

## Mk4 Fringe Plot



Amp. and Phase vs. time for each freq., 28 segs, 11 APs / seg (11.00 sec / seg.), time ticks 10 sec



	8640.00	8704.00	8768.00	8832.00	8896.00	8960.00	9024.00	Freq (MHz)	All
UL	0/299	0/299	0/299	0/299	0/299	0/299	0/299		
E:G	-18000~-15000	-18000~-14000	-18000~-13000	-18000~-17000	-18000~-16000	-18000~-15000	-18000~-14000		
E:G	65-143	96:86	-167~-176	-63~-9	38:114	125~-93	165:30		
E:G	0:0	0:0	0:0	0:0	0:0	0:0	0:0		
E:G	28: 28	36: 27	25: 24	27: 31	27: 29	25: 27	23: 25		
E	X8L	X7L	X6L	X5L	X4L	X3L	X2L		
G	X3L	X2L	X1L	X0L	X4L	X3L	X2L		
Group delay (usec)	6.07474040240E+02	6.07479802689E+02	6.07473651241E+02	6.07473651241E+02	6.07473651241E+02	6.07473651241E+02	6.07473651241E+02	3.89000E-04	+/- 7.3E-06
Sband delay (usec)	6.07479802689E+02	6.07479802689E+02	6.07479802689E+02	6.07479802689E+02	6.07479802689E+02	6.07479802689E+02	6.07479802689E+02	6.15145E-03	+/- 1.0E-04
Phase delay (usec)	6.07473651241E+02	6.07473651241E+02	6.07473651241E+02	6.07473651241E+02	6.07473651241E+02	6.07473651241E+02	6.07473651241E+02	3.92336E-06	+/- 2.2E-07
Delay rate (us/s)	-9.44554813859E-02	-9.44554813859E-02	-9.44554813859E-02	-9.44554813859E-02	-9.44554813859E-02	-9.44554813859E-02	-9.44554813859E-02	-3.68981E-07	+/- 1.2E-09
Total phase (deg)	137.0	137.0	137.0	137.0	137.0	137.0	137.0	12.2	+/- 0.7
pcal mode	NORMAL	NORMAL	NORMAL	NORMAL	NORMAL	NORMAL	NORMAL		
pcal rate	4.252E-08	-1.543E-07	4.252E-08	-1.543E-07	4.252E-08	-1.543E-07	4.252E-08		
Bits/sample	2	2	2	2	2	2	2		
Sample rate (MSamples)	64	64	64	64	64	64	64		
Data rate (Mbits)	896	896	896	896	896	896	896		
Flags	32	32	32	32	32	32	32		

Control file: cf\_3330 / Input file: /data/1330/133-1500/EG.uvmgdk Output file: Suppressed by test mode

EVN-10G Meeting June 21, 2010

# DDC Development (jon)

- Specs
  - Digital downconverter.
  - 2 IF inputs, each 512 MHz wide.
  - 2 x 4 sub-bands from initial PFB, each 128 MHz.
  - 16 digital filters, any sub-band available to any filter.
    - Filter bandwidths 62.5 kHz – 128 MHz.
- Status
  - Under development.
  - Replacing all elements of PFB personality except:
    - Sampler input interface.
    - VSI (Mark 5B) formatter.
    - 10 Gigabit Ethernet output interface.
    - PPC infrastructure.
  - Initial versions of most new blocks complete.



# Other VLBA Upgrade Topics (jon)

- New VLBA Station Control Software
  - Will be installed with RDBE and Mark 5C.
  - Will initially control only those new elements.
  - Status: “Current”
    - Program infrastructure complete and operational.
    - All currently specified tasks/commands/responses implemented.
    - Incorporation of new elements expected to be easy.
- DiFX Software Correlator
  - In operational use since end of 2009.
- Recording Media & Correlation Processors
  - Funding granted by NSF for upgrades to support full-time observing at 2 Gbps.

# Mark5C (chet)

- DRS-0.9 Status
  - Packaged
    - Debian (Haystack)
      - Available June 23
    - Red Hat (NRAO)
  - 2Gbps / Bank Mode / Mark5B emulation Mode
  - New Directory Structure
    - (memo series)

# Mark5C (chet)

- DRS\_utils
  - Clients
    - Graphical
    - Command line
  - Streamstor utilities
    - SSErase, SSReset,
  - 5B packet checking utility
    - PacketChecker

# Mark5C (chet)

- FuseMk5 Modifications
  - New directory structure support
  - Coordinate with Jan Wagner
- Mark5C misc.
  - Debian Lenny (2.6.26-2-686 kernel)
    - Base install being created (iso image)
  - SDK 9.0
    - 32 bit kernel support
    - Large disk support
    - Debian package under test

# Mark5C (chet)

- DRS-1.0
  - Additional features to be added:
    - Vdif support
      - User Directory Changes
    - 64 bit kernel support (SDK9.1)
      - Expect from Conduant mid August
    - 4Gbps / Non-Bank Mode
  - Target release date -> September

# Mark5 (chet)

- SDK-8 to SDK-9 issues
  - SDK9 is not backward compatible
    - Cannot be read with SDK8 machines
  - Can read SDK6/7/8 recordings
  - Requires flashing for 5B+ systems
    - To support larger disks
- MarkIV Correlator
  - Version under test on Mark5B+
  - Have not tested with Mark5A units

# Mark5 (chet)

- End Stations
  - Under consideration to support SDK9
    - Mark5A's
    - Mark5B's
  - Requires modification to Mark5A/B code
    - Variable declaration
    - Some XLR function calls modification
    - Debuggery (print outs)

# Mark5

- SDK9 discussion point
  - Interest for upgrading to SDK9?
  - Support for larger disks?
  - New hardware?



# Questions / Comments?