Cryogenic Performance of NGC 35nm InP Low Noise Amplifiers



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Atacama Large Millimeter/submillimeter Array Expanded Very Large Array Robert C. Byrd Green Bank Telescope Very Long Baseline Array







- Wafer run complete 1/15/2008
- Chip Dimension: 2.1mm x 0.8mm



On-chip Measurements

On-wafer, T=297K Gain (dB) R13C02M0 - R15C02M0 Frequency (GHz)

EBLNA81 (VG=+0.3V, VD=1.2V)

• G_m increased in simulation (from 1950 to 2500 mS/mm) to match measured performance



Cryogenic Performance of 35nm InP LNAs

On-Chip Noise Measurement





On-chip Noise Measurement





WR-I2 LNA Module



Same MDM-15 pinout as CDL LNAs

WR-I2 LNA Module

Cryogenic Performance of 35nm InP LNAs

S21

Noise

EBLNA81 T=297K, Vd=0.8V, Id=21mA

EBLNA81 Vd=0.8V

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Vd=0.8V, Id=7mA/stage

NRAO

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- Simulation: Gm=2500mS/mm, Igs=0, Tdrain=1400
- Pdiss = 5.55mW

NRAO

35nm 3-stage LNA (EBLNA81)

• Blue trace shows noise for minimum power dissipation: Vd1=0.35V, Vd23=0.5V, Id=4.5mA -> Pdiss = 2.06mW

Pinchoff Characteristics

Cryogenic Performance of 35nm InP LNAs

Why the frequency shift cold?

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EBLNA81 (T=297K,Vd=0.8V,Id23=7mA)

• Hypothesis: Cgs(Vgs) is causing frequency shift

Revised cryogenic model for parasitics

EBLNA81 Vd=0.8V

• Change in S21 also modeled well by decrease in Cgs

Revised cryogenic model for parasitics

• Id1=1.5mA

 Simulation: gm1=33.6mS, gm23=66.6mS, Cgs1=12.6fF (versus 17.5fF in original model)

Revised cryogenic model for parasitics

• Simulation: Gm1=64mS, Gm23=90mS, Td1=1400K, Td23=2800K, Cgs1=12.6fF (compared to 17.5fF original)

EBLNA81B: Retuned for 67-90 GHz

Cryogenic Performance of 35nm InP LNAs

EBLNAW+: Cover full 68-116 GHz band

MMLNI00: Cover full 68-116 GHz band

EBLNAW0: A "Tunable" MMIC LNA

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Questions / Discussion Points

- Is the process repeatable?
- These results are with 70% channel, what do they look like with 100% channel (higher gm)?
- Operation at 4K
- Ultimate limit for W-band LNA noise temperature
- Comparison to SIS development

