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Prototype Hardware

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1 Document information

Document name: UniBoard² – Prototype hardware

Type: Prototype – Report

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1.1 Dissemination Level

Dissemination Level		
PU	Public	
PP	Restricted to other programme participants (including the Commission Services)	
RE	Restricted to a group specified by the consortium (including the Commission Services)	X
CO	Confidential, only for members of the consortium (including the Commission Services)	

1.2 Content

1	Document information	2
1.1	Dissemination Level	2
1.2	Content	3
2	Introduction	4
3	Images	4

2 Introduction

The UniBoard² JRA set out to create an FPGA-based, generic, scalable, high-performance computing platform for Radio Astronomy, along with a number of firmware personalities, like a correlator, beam former and a digital receiver.

During the hardware development, a single prototype board was designed and produced and delivered by Neways, the manufacturing company, in May 2015. An intensive period of testing followed, after which the revised design was sent to Neways in August 2015 in order to start up a production run of 7 boards.

The design of the board and of the various firmware applications are explained in detail in the following deliverable documents:

- D8.2: Hardware Design Document
- D8.3: Firmware Design Document: EVN Correlator and SKA Low Frequency Channeliser
- D8.4: Firmware Design Document: Digital Receiver
- D8.5: Firmware Design Document: Beam Former
- D8.6: Firmware Design Document: Pulsar Binning
- D8.7: Firmware Design Document: RFI Mitigation

3 Images



Figure 1: hardware engineer Sjouke Zwier checks the PCB during the intermediate stages of the assembly



Figure 2: chief designer Gijs Schoonderbeek checking the finer details



Figure 3: first tests at the lab in Dwingeloo

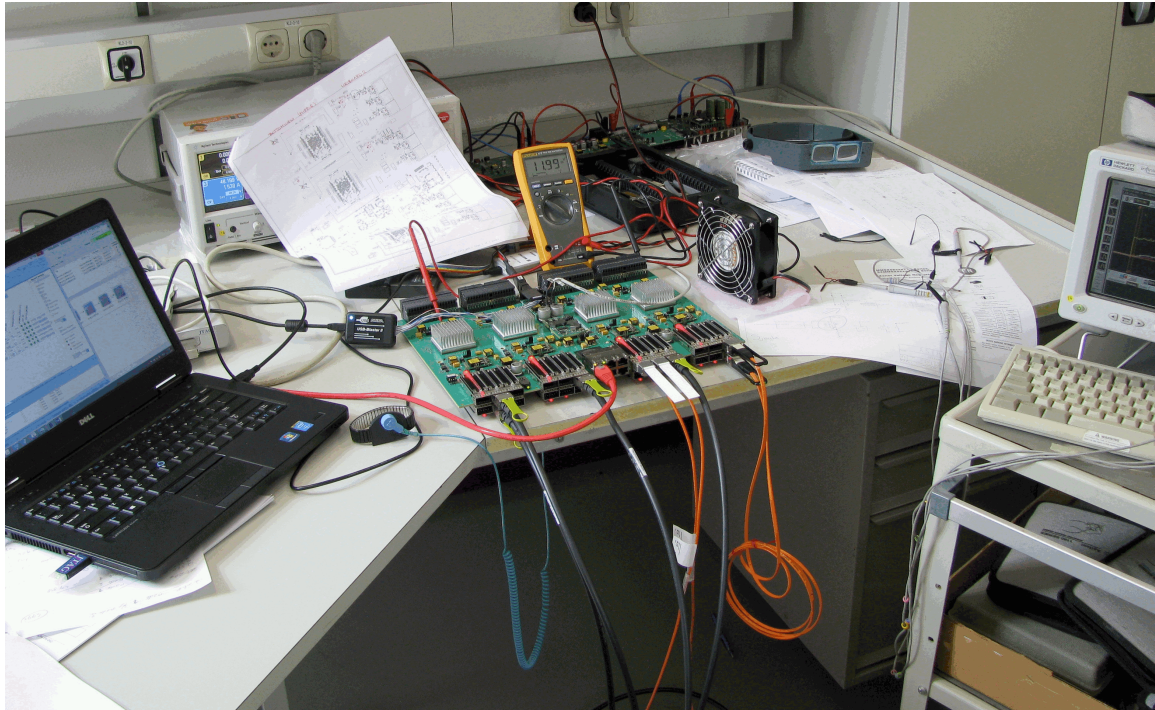


Figure 4: first (LED) light

Personal Message ... (ASTRON/JIVE ... V Schoppende c... (ASTRON | AST... (ASTRON JIVE ... Participants - ... jrasuniboard2... Rechtsposi... Doodle: Filat0 ... Task 34 Work ... EBV NEWS... jrasuniboard2... +

blog.ebv.com/breaking-the-1tbps-barrier-with-uniboard2/ breaking the 1Tbps barrier with uniboard

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BREAKING THE 1TBPS BARRIER WITH UNIBOARD2

POSTED ON 30 JULY 2015 BY KAI SCHMIDT IN LIFESTYLE, UNCATEGORIZED

Breaking The 1Tbps Barrier With UniBoard2

Recently several engineers broke the 1 Tbps barrier within the UniBoard2 project!

UniBoard2, an activity which is part of the RadioNet3 project aims to create a FPGA-based, generic, scalable, high-performance computing platform for radio-astronomical applications. The innovative re-designed second generation builds upon the experience obtained through the UniBoard project and will be ready for the next generation of astronomical instruments (notably the SKA), at the end of 2015.

Lately several engineers pushed the boundaries of what's possible breaking the 1 Tbps barrier with the UniBoard2 and submitted the picture of the victorious team behind the success to the ASTRON JIVE Daily Image (AJDI) archive. AJDI is a family chronicle of the sister institutes ASTRON and JIVE that proudly presents their scientific and technical successes and the people behind them.

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Figure 5: making headlines

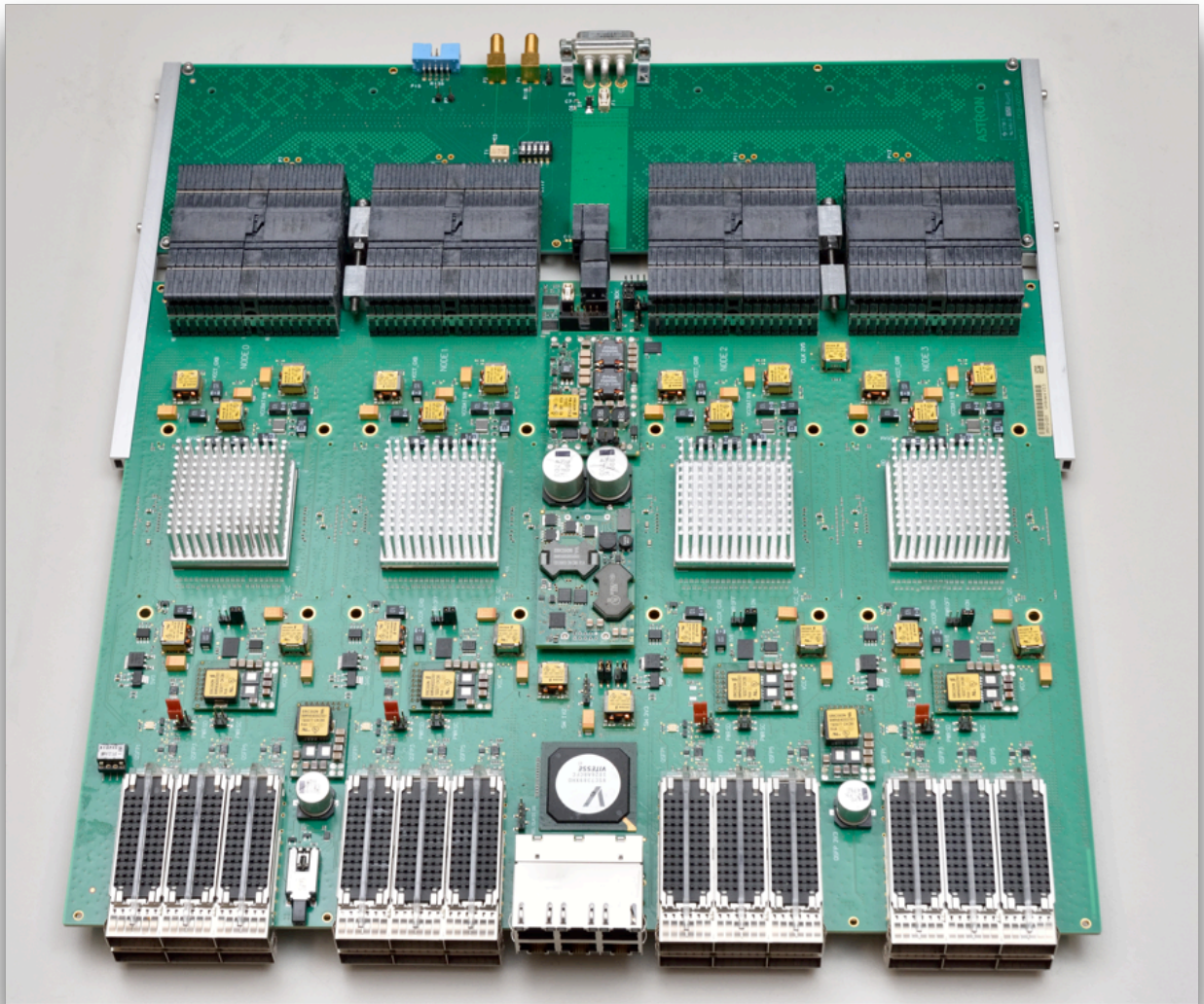


Figure 6: prototype UniBoard² with cooling blocks mounted on the four FPGAs and an extension test board connected to the backplane connectors

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