UniBoard Rev 1.0

hardware point of view

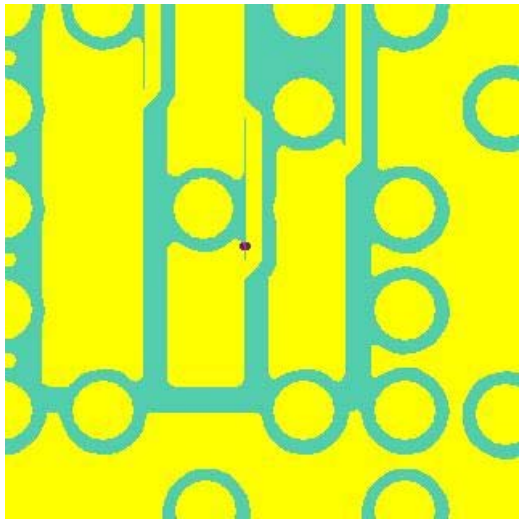
Work done since last meeting

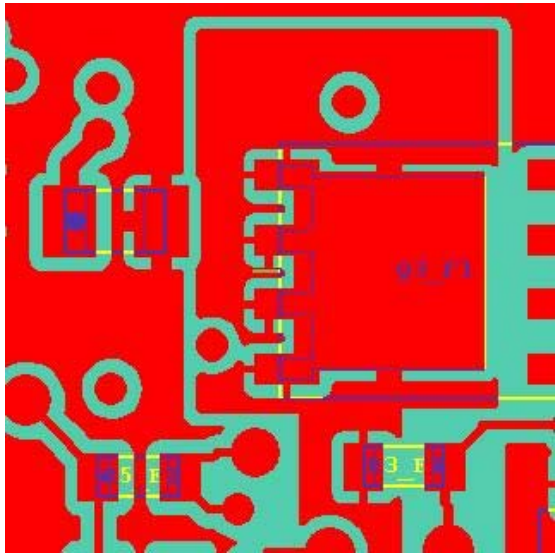
- Optimize design for production
- Production of UniBoard (Neways)
- Testing the board
- Made 10G break out board (XGB)
- Design housing for UniBoard / XGB
- Memory and ADC test boards made
- Start with updating design for rev 2.0

Optimize design for production

DFM for:

- Preventing PCB production errors
- Reducing assembly problems like:
  - Wrong shapes
  - tomb stones

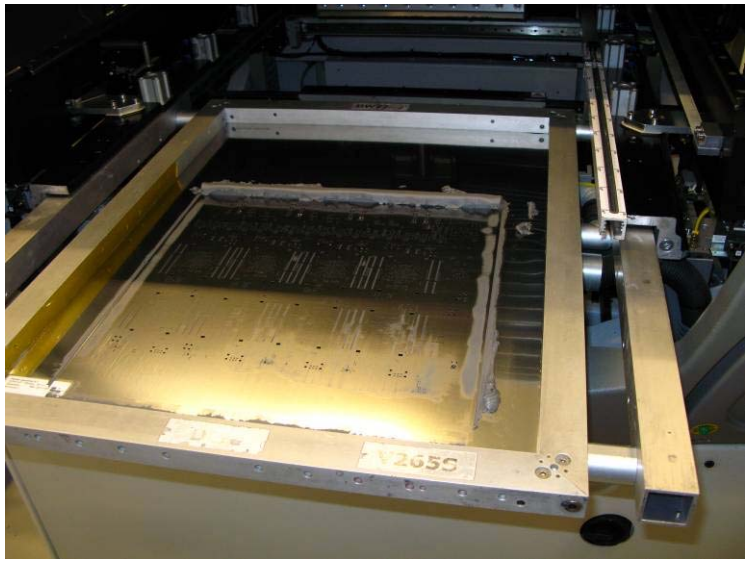


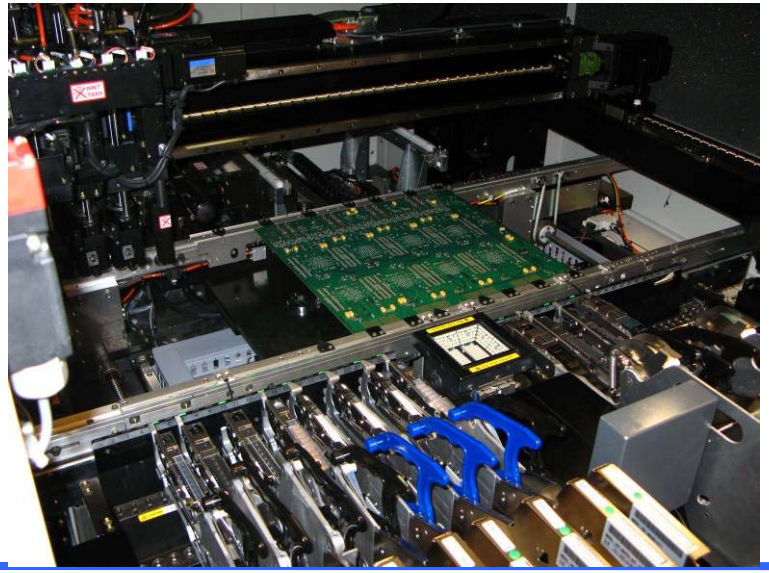


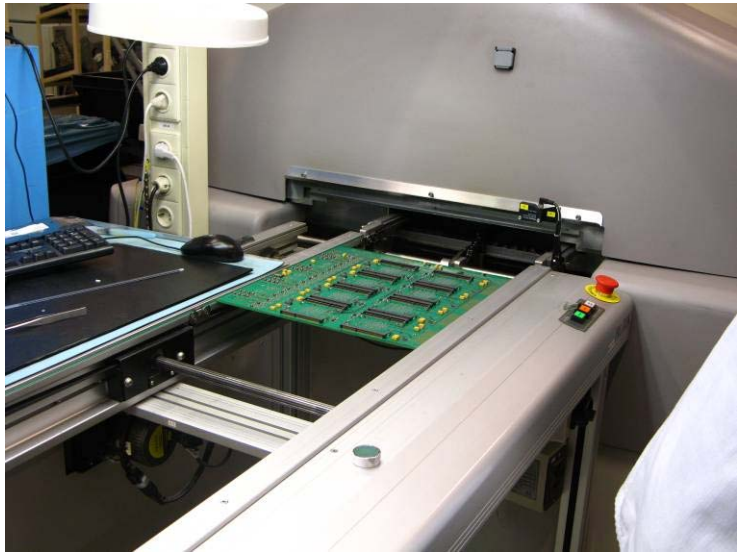
Result:

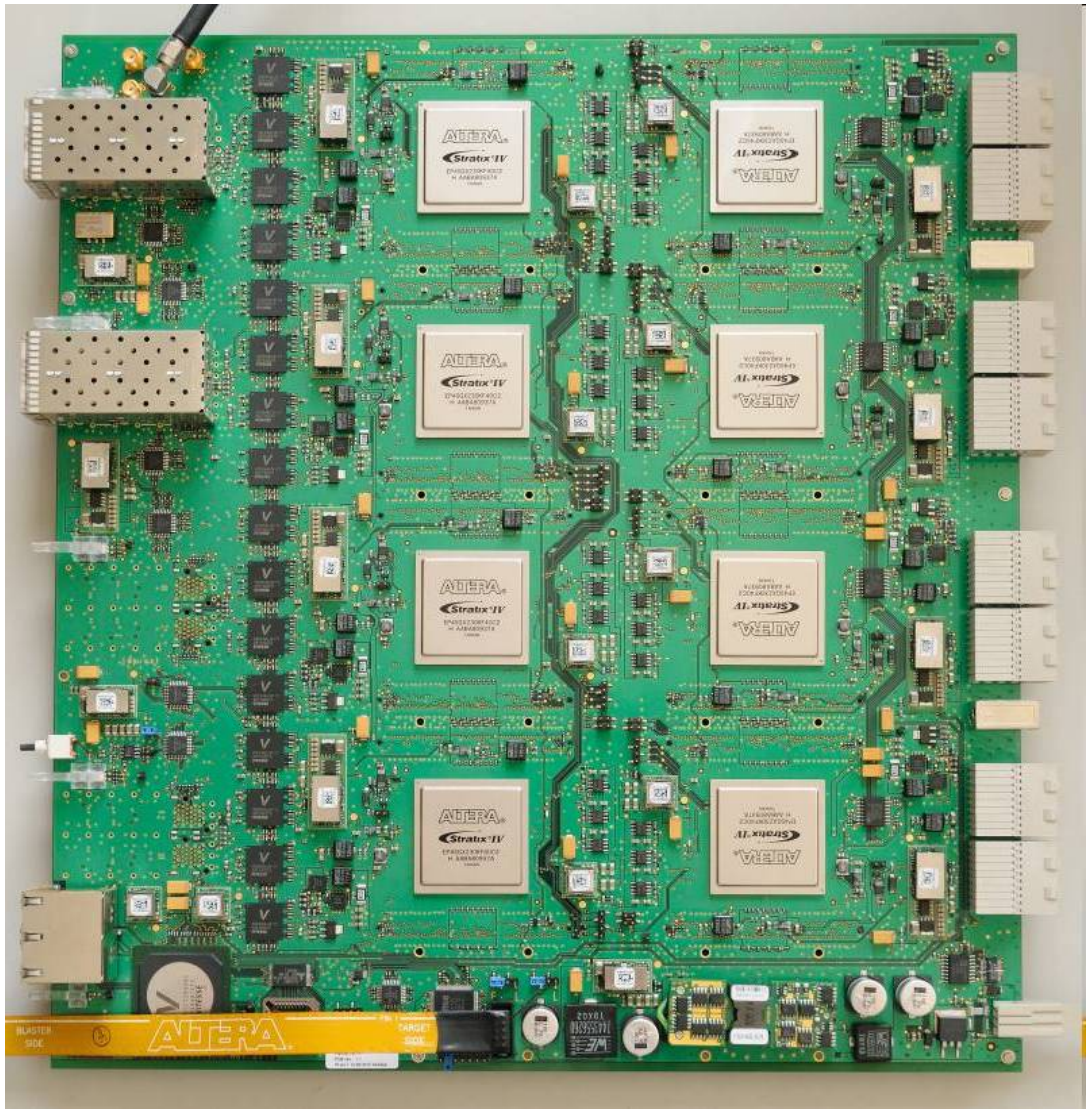
- Only one wrong footprint (of 138 different parts)

UniBoard Production









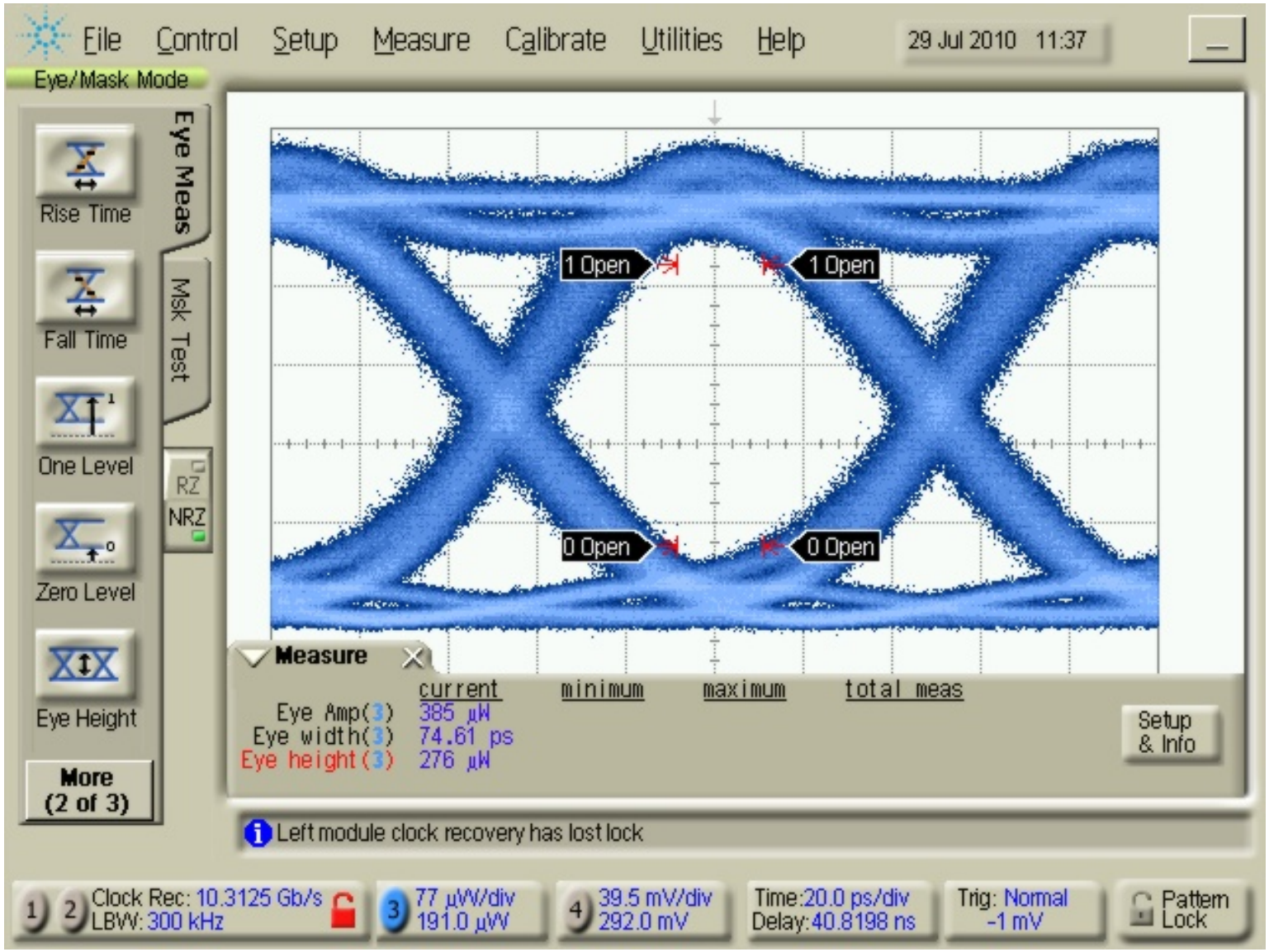
Test Results

- Boundary scan
- DDR3 tested up to 1033MT/s
- Inner FPGA interfaces tested up to 6.5Gbps
- IO interfaces tested up to 10Gbps with optical interfaces
- ADC interfaces tested up to 200MSPS (due to limited of test fixture)
- GbE control tested (unmanaged) hardware o.k. software need update.

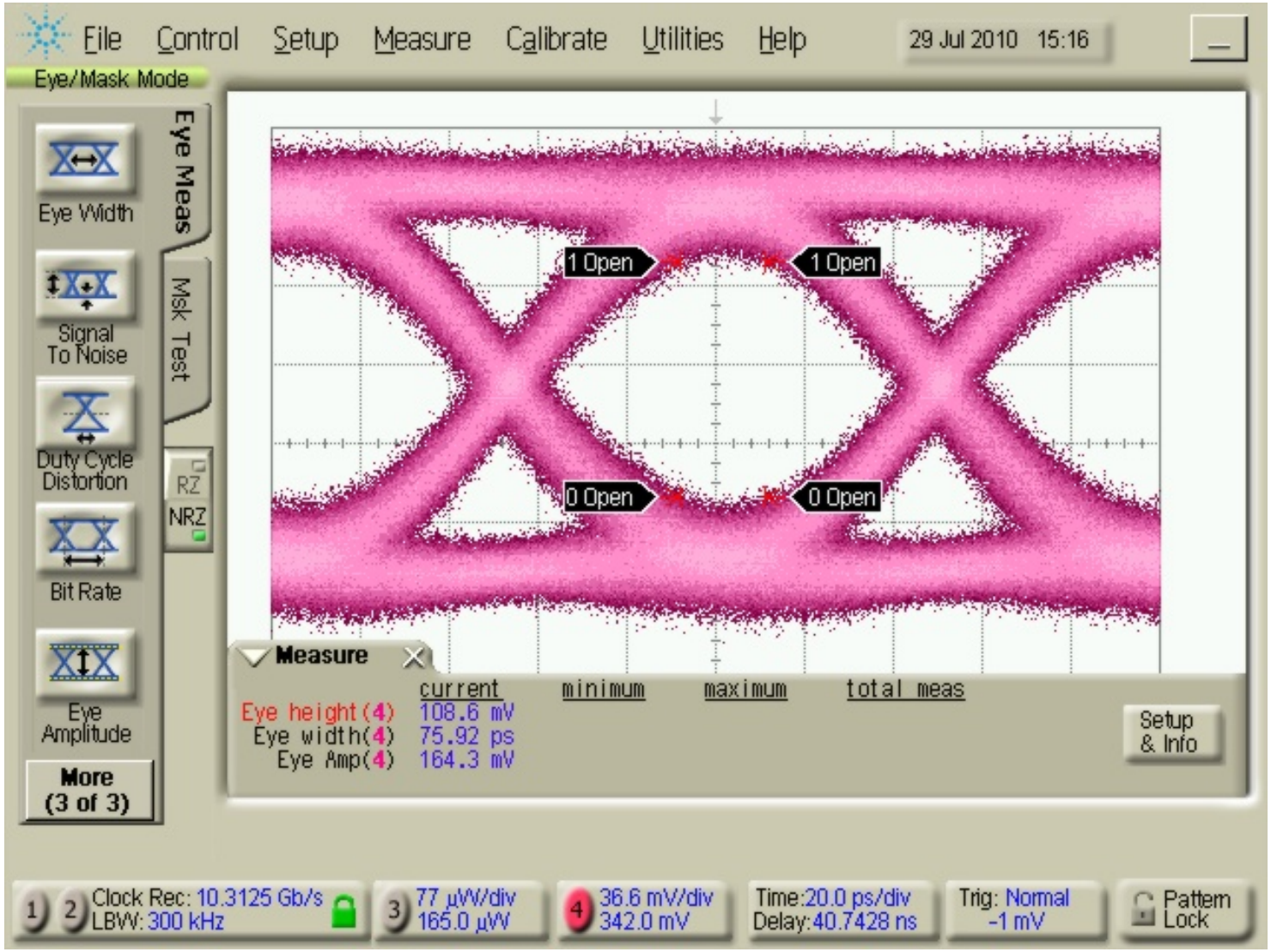
Known Issues

- Small PCB issue's
  - 1 shape
  - Different values (termination and power settings)
- DDR3 power supply not capable of max. current
- Transceivers Power
  - Not sufficient output power for direct attachment cabling
  - Tx, Rx swap in SFP+ slot 3
- FPGA
  - DDR pinning lost connection
- Ethernet switch
  - Memory size for managed switch
  - More testing needed

Optical Measurement results

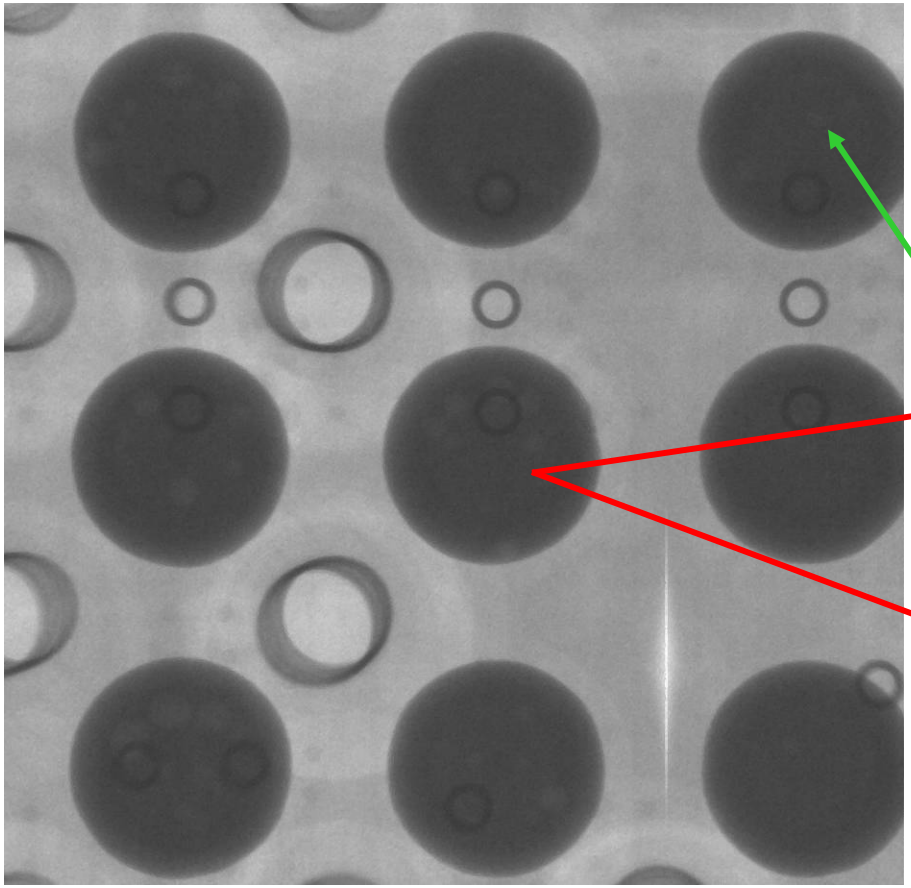


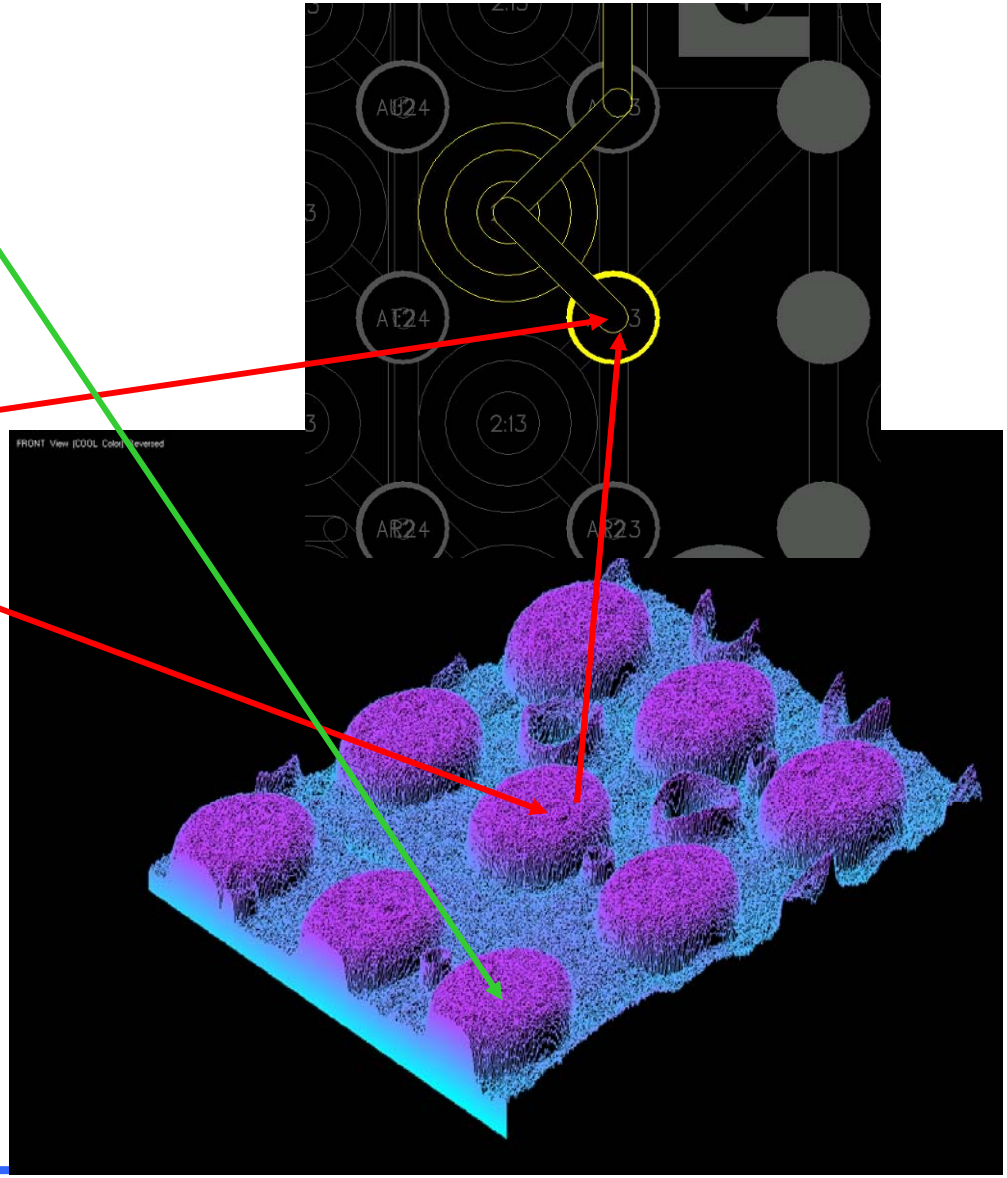
S.E. Copper measurement result



DDR3 eye pattern

X-Ray scan on memory lines





- BN 2 pin AT23
- MBII A4

Boundary scan on memory lines

TTR - Microsoft Internet Explorer

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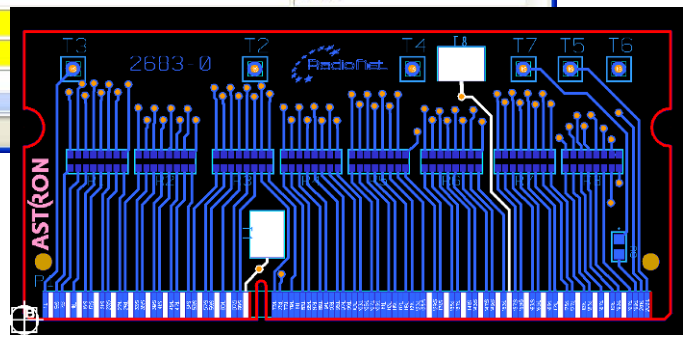
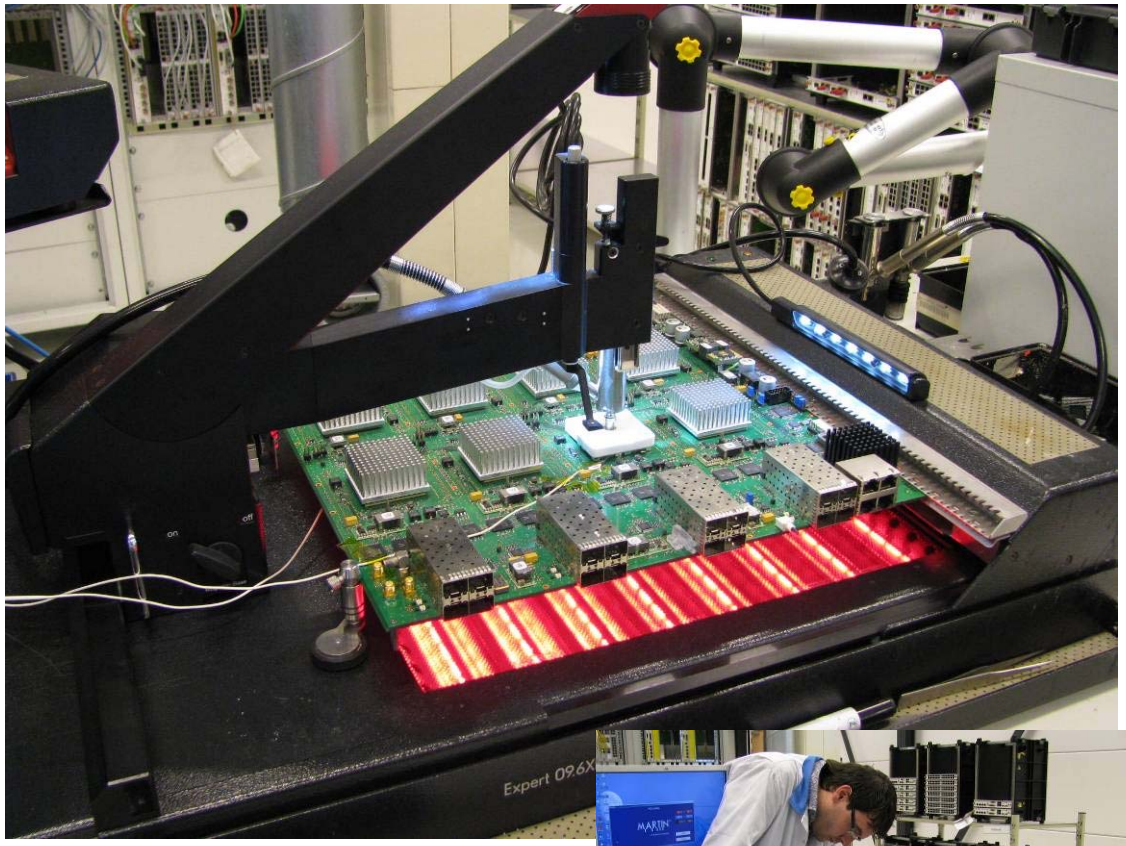
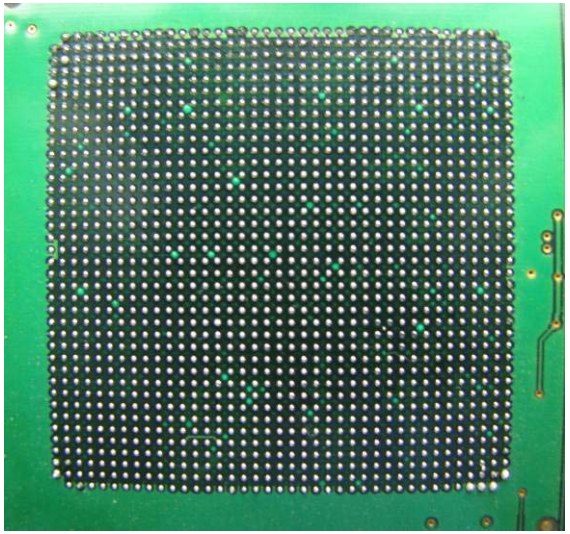
	MERGED_NET_MB_II_A4_130_unib_220310_v6_1	MERGED_NET_MB_II_DQ46_133_unib_220310_v6_1	MERGED_NET_MB_II_DQ46_159_unib_220310_v6_1	MERGED_NET_MB_II_S_NO
1	H1Z1	H1Z1	H1Z1	H1Z1
2	L0Z1	L0Z1	L0Z1	L0Z1
3	Z0L0	Z0L0	Z0L0	Z0L0
4	Z1H1	Z0H1	Z1H1	Z1H1
5	H1Z1	H1Z1	H1Z1	H1Z1
6	H1Z1	H1Z1	H1Z1	H1Z1
7	L0Z1	L0Z1	L0Z1	L0Z1
8	L0Z1	L0Z0	L0Z1	L0Z1
9	H1Z1	H1Z0	H1Z1	H1Z1
10	H1Z1	H1Z1	H1Z1	H1Z1
11	L0Z1	L0Z1	L0Z1	L0Z1
12	L0Z1	L0Z0	L0Z1	L0Z1
13	H1Z1	H1Z0	H1Z1	H1Z1
14	H1Z1	H1Z1	H1Z1	H1Z1
15	L0Z1	L0Z1	L0Z1	
16	L0Z1	L0Z0	L0Z1	
17	H1Z1	H1Z0	H1Z1	

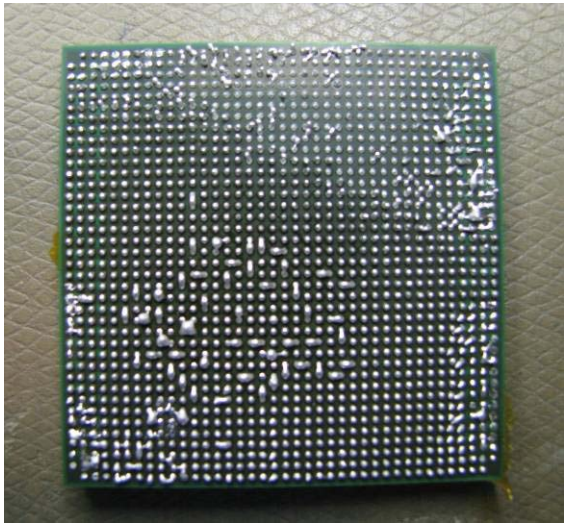
Done



Removing of FPGA



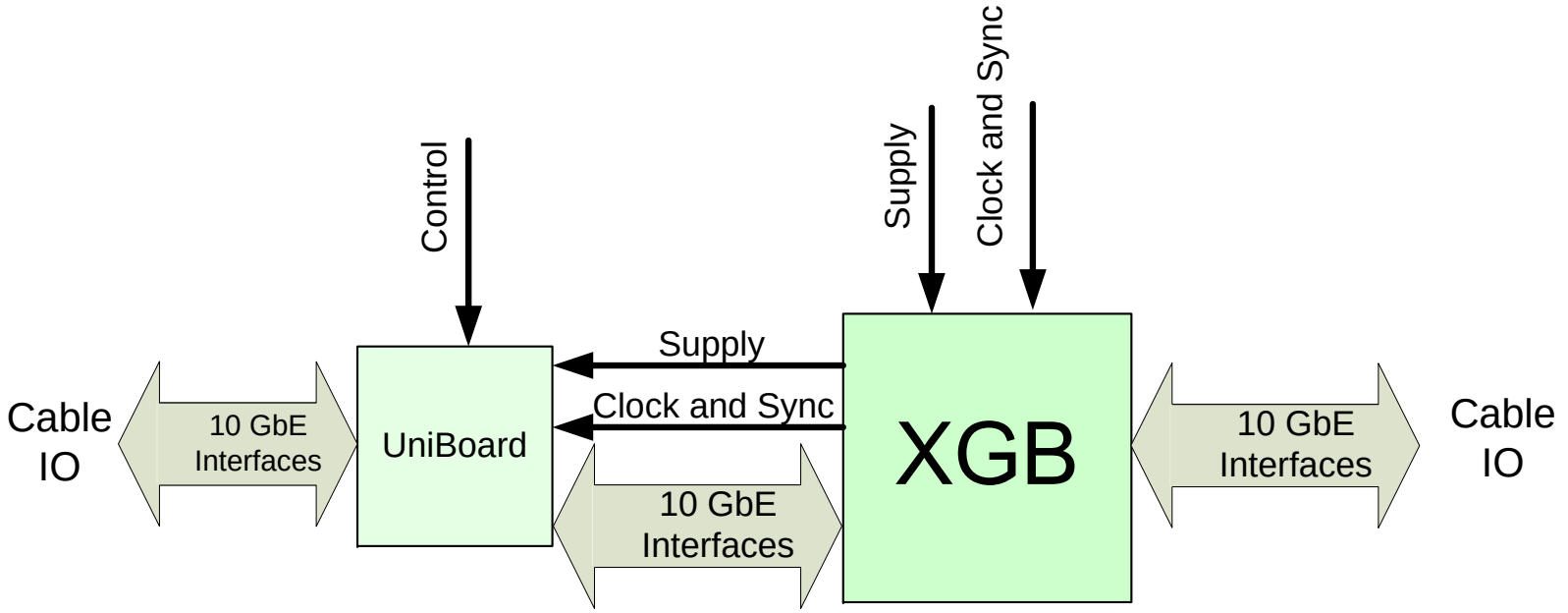


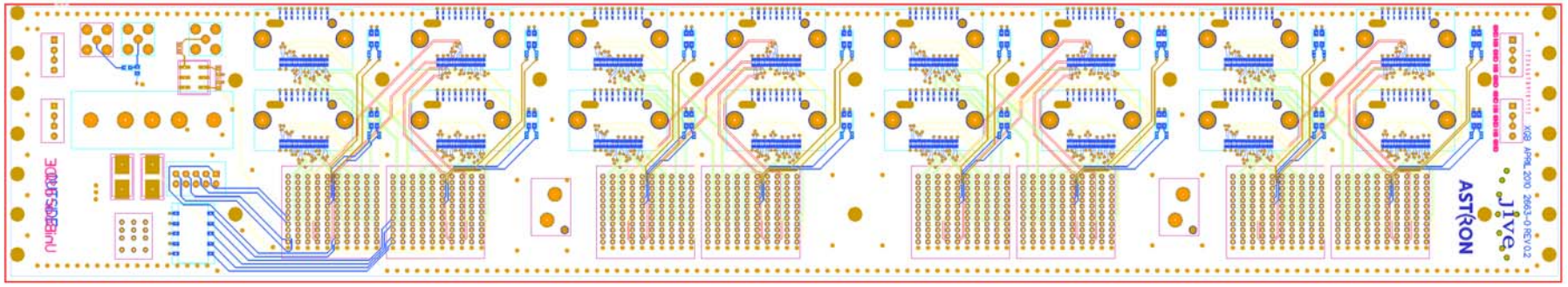


Changes for rev 2.0

- DDR3 power supply (setting of the SMPS)
- Ethernet switch, unmanaged
- Remove Tx Rx swap in SFP+
- Removing small errors

XGB 10Gig Breakout board

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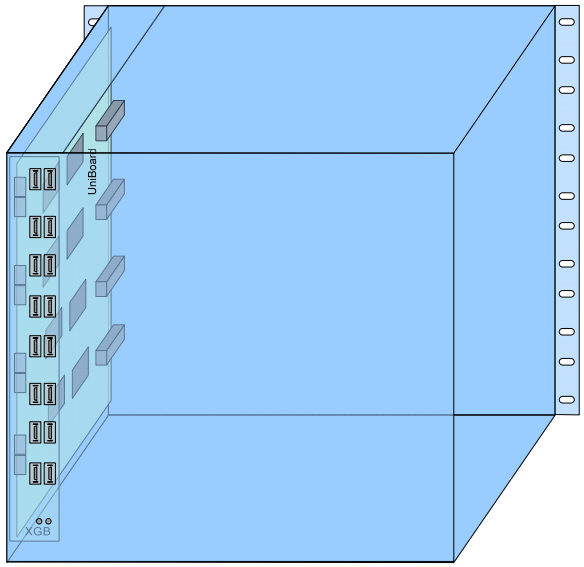
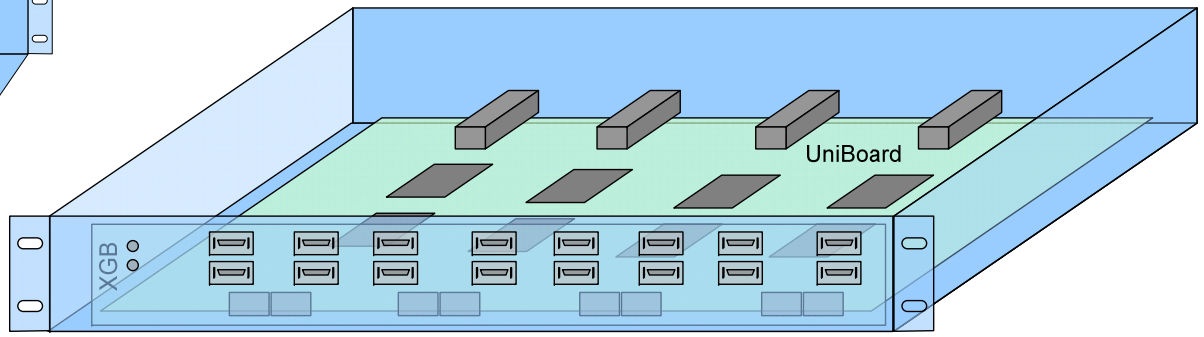
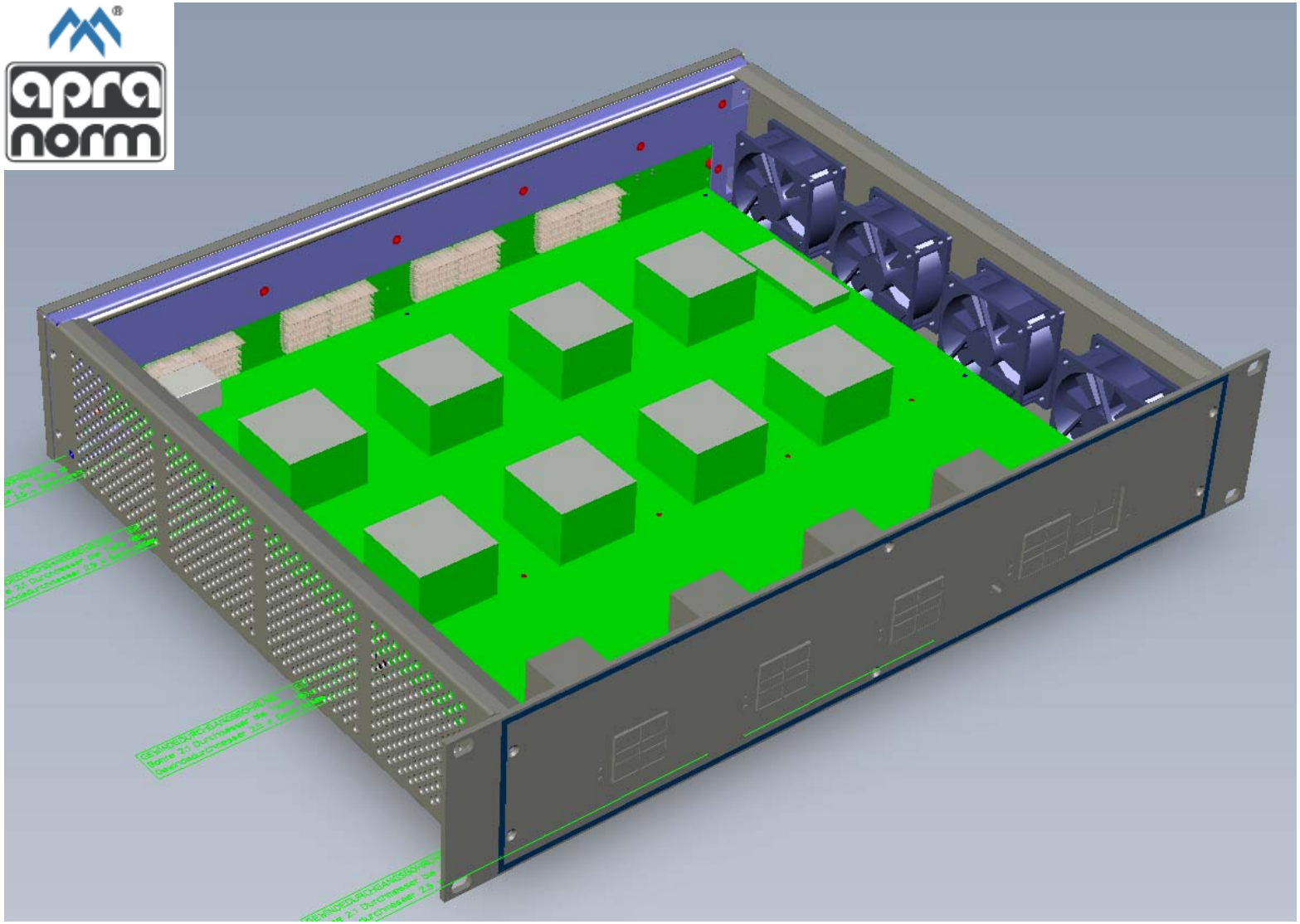
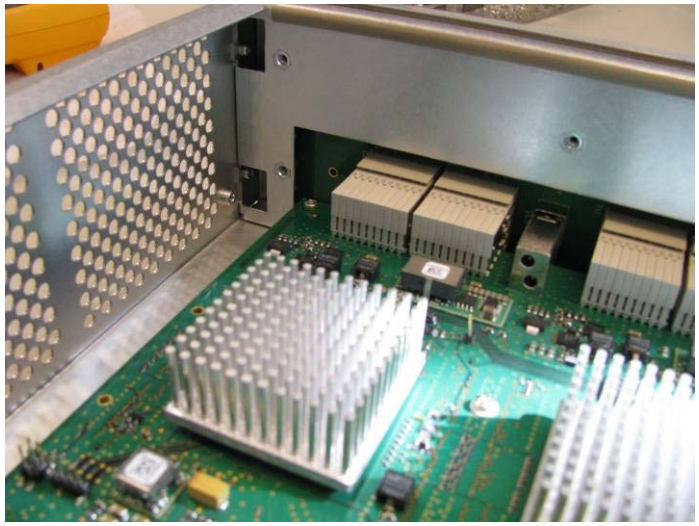
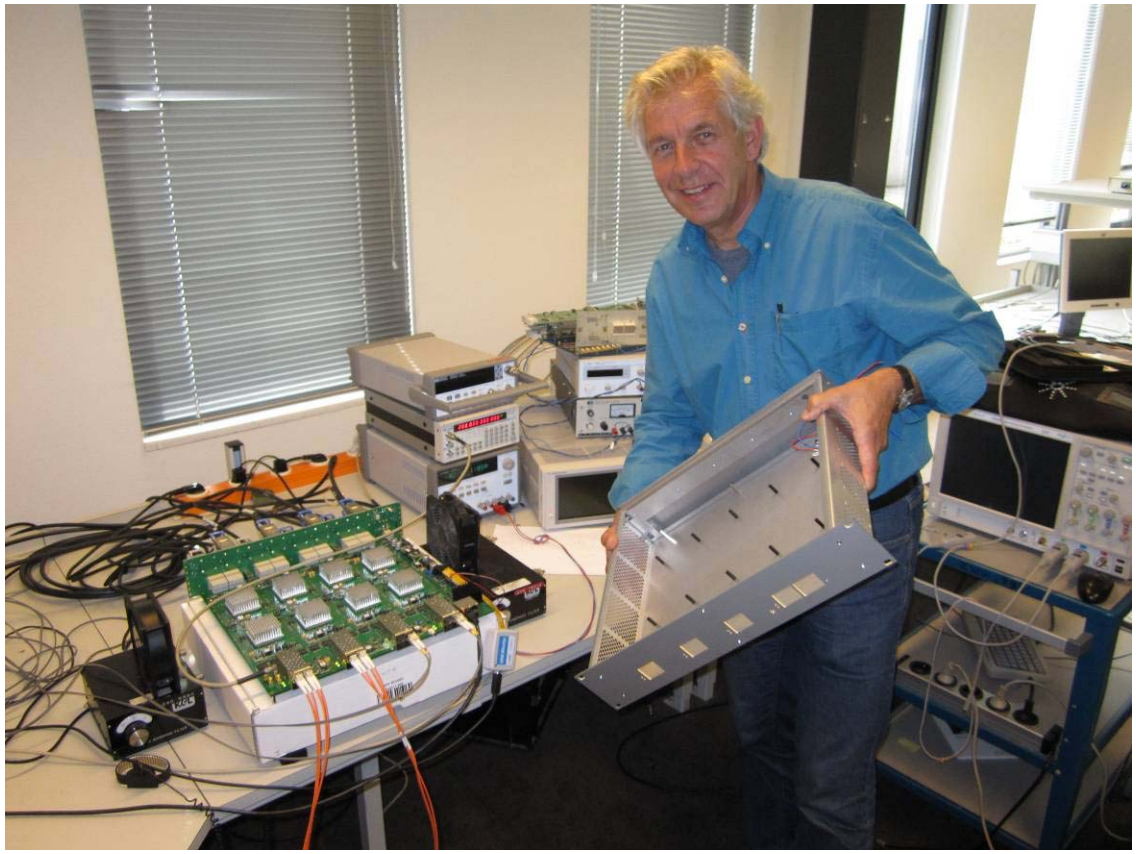

UniBoard
XGB

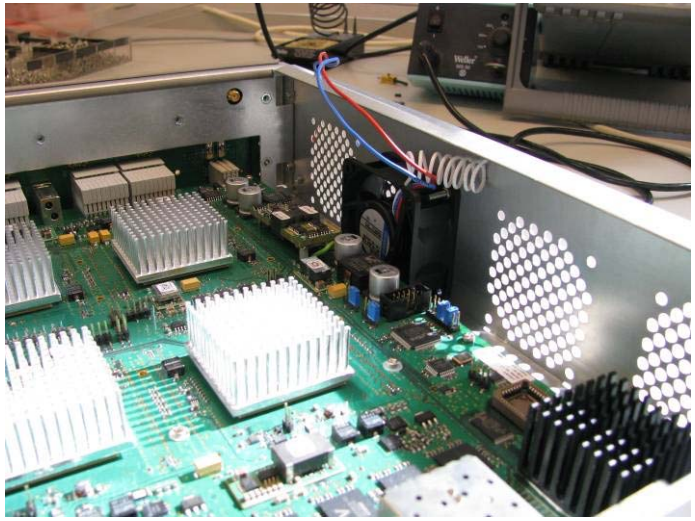

UniBoard
XGB

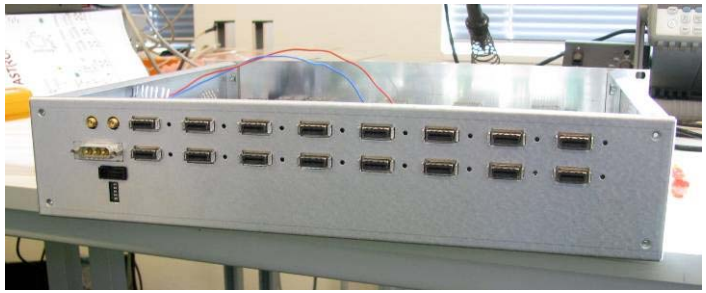


UniBoard 2HE Housing









Hardware

* UniBoard for EVN: Block diagram and analysis. Gijs Schoonderbeek, 13-3-2009
* UniBoard hardware design. Gijs Schoonderbeek, Sjouke Zwier, 29-01-2010
* UniBoard Schematic. Gijs Schoonderbeek, Sjouke Zwier, 29-01-2010
* PPT for Schematic Review. Gijs Schoonderbeek, Sjouke Zwier, 07-07-2009
* UniBoard PCB (preplacement) Sjouke Zwier / Gijs Schoonderbeek. 15-09-2009
* UniBoard Test Description. Sjouke Zwier / Gijs Schoonderbeek. 15-04-2010
* UniBoard Board Description. Sjouke Zwier / Gijs Schoonderbeek. 14-07-2010
* XGB hardware design document. Gijs Schoonderbeek, Sjouke Zwier, 07-04-2010
* XGB Schematic. Sjouke Zwier / Gijs Schoonderbeek 14-04-2010
* XGB PCB Overview. Sjouke Zwier / Gijs Schoonderbeek 14-04-2010
* UniBoard/XGB housing Sjouke Zwier / Gijs Schoonderbeek 07-07-2010

Description which tests will be done during production

Description of board, connectors and other non firmware issues

http://www.radionet-eu.org/fp7wiki/doku.php?id=jra:uniboard:documents

- Finalize Redesign
  - Find cause of DDR connection problem
  - Finish testing
  - Remove errors in rev 1.0 (update started)
- Update XGB
- Start production UniBoard
- Start production of housing
- Prepare for production test

Plans for UniBoard Rev 3.0

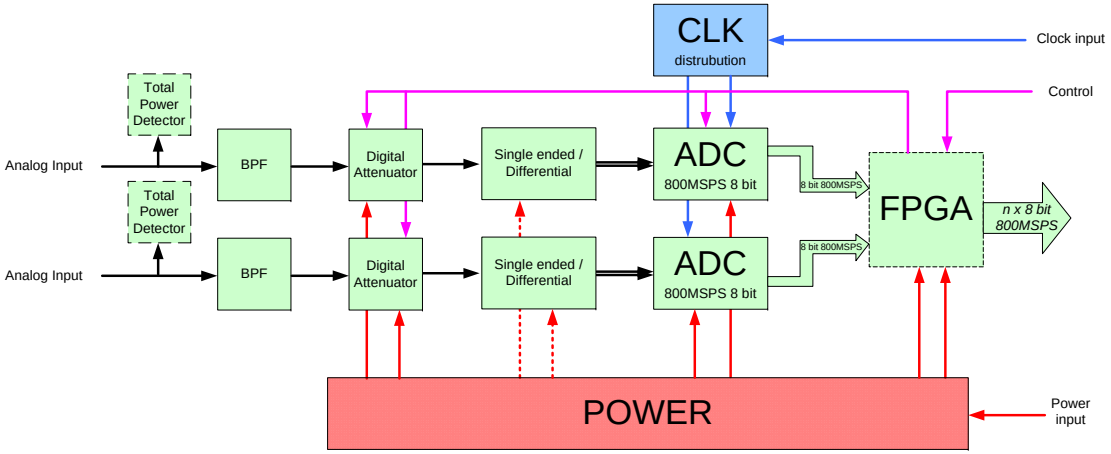
- Transceiver change to different type
- Backplane ON/OFF

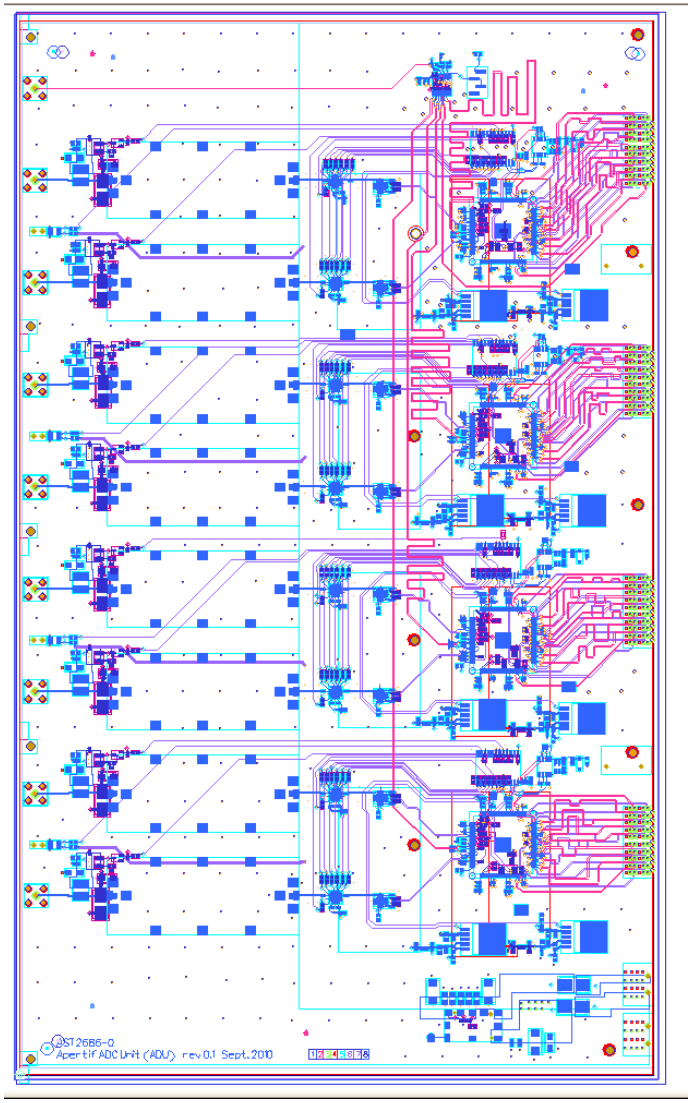
Subrack with ADC for Apertif

- 4 UniBoards
- 8 ADC-boards (ADU)
- 1 power and clock board (PAC)
- 1 backplane

ADU

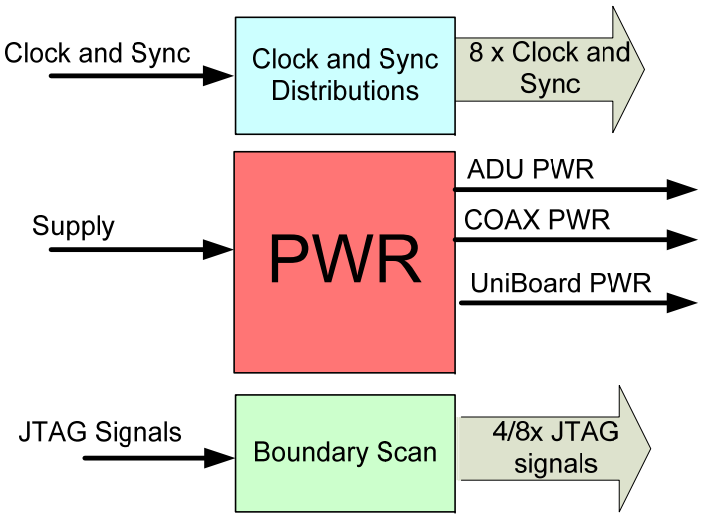
- National Semiconductor ADC08D1200 800MSPS 8 bit
- 8 channels per board
- 400-800MHz filters
- Ready for power over coax
- Est. <1W / channel

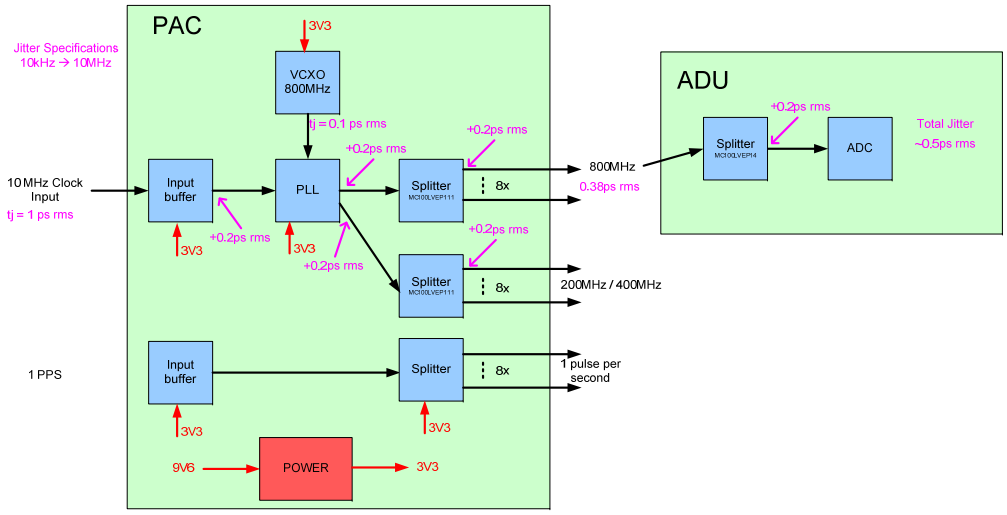




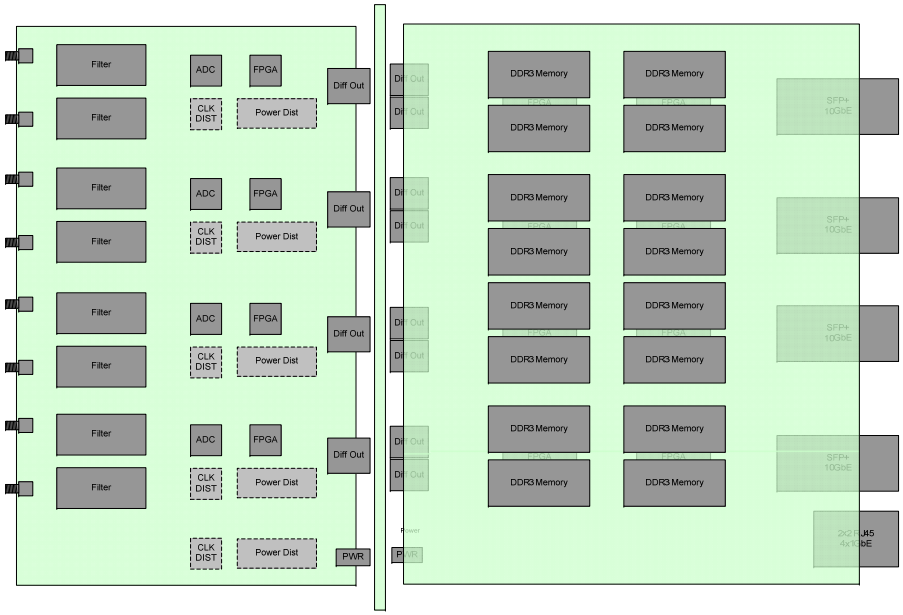
PAC

- Clock distribution to ADCs and UniBoards
- Power distribution
- Boundary scan signal distribution





Astron UniBoard plans



Planning other boards

- Finish UniBoard and XGB

- ADU current in production
- PAC specification finish design started
- Backplane Q1 2011 in production